DATASHEET
FOR
64M BIT SPI NOR FLASH

BY25Q64AL

Features

- **Serial Peripheral Interface**
  - Standard SPI: SCLK, /CS, SI, SO, /WP, /HOLD
  - Dual SPI: SCLK, /CS, IO0, IO1, /WP, /HOLD
  - Quad SPI: SCLK, /CS, IO0, IO1, IO2, IO3
  - QPI: SCLK, /CS, IO0, IO1, IO2, IO3
  - Software & Hardware Reset
- **Read**
  - Normal Read (Serial): 50MHz clock rate
  - Fast Read (Serial): 108MHz clock rate
  - Dual/Quad (Multi-I/O) Read: 108MHz clock rate
- **Program**
  - Serial-input Page Program up to 256bytes
  - Quad-input Page Program up to 256bytes
  - Program Suspend and Resume
- **Erase**
  - Block erase (64/32 KB)
  - Sector erase (4 KB)
  - Chip erase
  - Erase Suspend and Resume
- **Program/Erase Speed**
  - Page Program time: 0.7ms typical
  - Sector Erase time: 60ms typical
  - Block Erase time: 0.3/0.5s typical
  - Chip Erase time: 30s typical
- **Flexible Architecture**
  - Sector of 4K-byte
  - Block of 32/64K-byte
- **Low Power Consumption**
  - 25mA maximum active current
  - 5uA maximum power down current
- **Software/Hardware Write Protection**
  - 3x256-Byte Security Registers with OTP Lock
  - Enable/Disable protection with WP Pin
  - Write protect all/portion of memory via software
  - Top or Bottom, Sector or Block selection
- **Single Supply Voltage**
  - Full voltage range: 1.65~1.95V
- **Temperature Range**
  - Commercial (0℃ to +70℃)
  - Industrial (-40℃ to +85℃)
- **Cycling Endurance/Data Retention**
  - Typical 100k Program-Erase cycles on any sector
  - Typical 20-year data retention at +55℃

Contents

1. Description

The BY25Q64AL is 64M-bit Serial Peripheral Interface(SPI) Flash memory, and support the standard Serial Peripheral Interface (SPI), Dual/Quad I/O SPI as well as 2-clocks instruction cycle Quad Peripheral Interface (QPI): Serial Clock, Chip Select, Serial Data I/O0 (DI), I/O1 (DO), I/O2 (/WP), and I/O3 (/HOLD). SPI clock frequencies of up to 108MHz are supported allowing equivalent clock rates of 216MHz (108MHz x 2) for Dual I/O and 432MHz (108MHzx4) for Quad I/O when using the Fast Read Dual/Quad and QPI instructions. These transfer rates can outperform standard Asynchronous 8 and 16-bit Parallel Flash memories. The Continuous Read Mode allows for efficient memory access with as few as 8-clocks of instruction-overhead to read a 24-bit address, allowing true XIP (execute in place) operation. The device uses a single low voltage power supply, ranging from 1.65 Volt to 1.95 Volt.

Additionally, the device supports JEDEC standard manufacturer and device ID, a 128-bit Unique Serial Number and three 256-bytes Security Registers.

BYTe Semiconductor offers an 8-pin SOP8 208mil package, an 8-pad WSON 6x5-mm package, and other special order packages. Please contact BYTe Semiconductor for ordering information.

Figure 1.1. Logic diagram

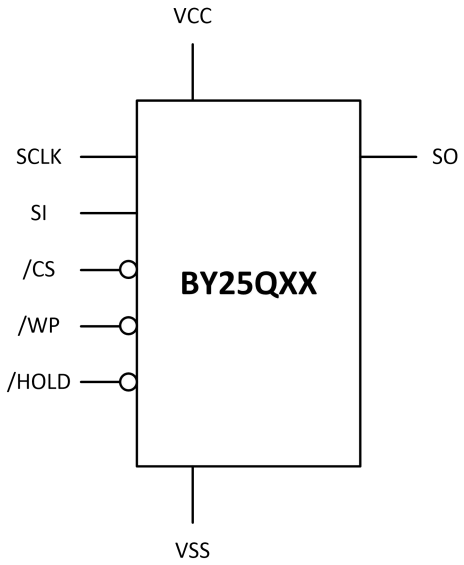


Figure 1.2. Pin Configuration SOP8 208-mil

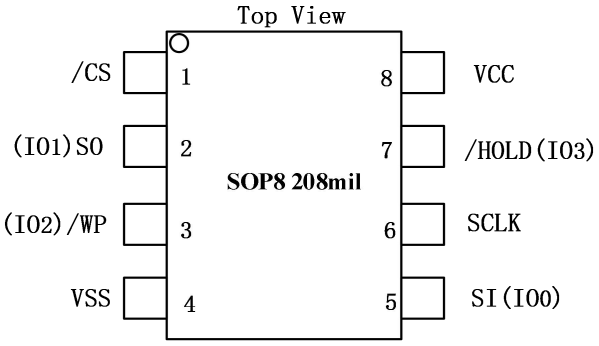
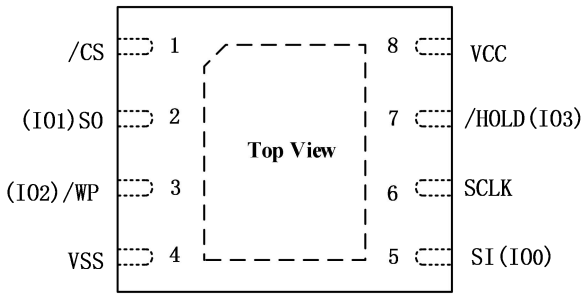


Figure 1.3. Pin Configuration WSON 6x5-mm



2. Signal Description

During all operations, VCC must be held stable and within the specified valid range: VCC(min) to VCC(max).

All of the input and output signals must be held High or Low (according to voltages of VIH, VOH, VIL or VOL, see Section 8.4, *DC Electrical Characteristics*). These signals are described next.

2.1 Input/Output Summary

Table 1. Signal Names

Pin Name	I/O	Description
/CS	I	Chip Select
SO (IO1)	I/O	Serial Output for single bit data Instructions. IO1 for Dual or Quad Instructions.
/WP (IO2)	I/O	Write Protect for single bit or Dual data Instructions. IO2 for Quad mode. This signal has an internal pull-up resistor and may be left unconnected in the host system if not used for Quad Instructions.
VSS		Ground
SI (IO0)	I/O	Serial Input for single bit data Instructions. IO0 for Dual or Quad Instructions.
SCLK	I	Serial Clock
/HOLD (IO3)	I/O	Hold (pause) serial transfer for single bit or Dual data Instructions. IO3 for Quad mode. This signal has an internal pull-up resistor and may be left unconnected in the host system if not used for Quad Instructions.
VCC		Core and I/O Power Supply

2.2 Chip Select (/CS)

The chip select signal indicates when an instruction for the device is in process and the other signals are relevant for the memory device. When the /CS signal is at the logic high state, the device is not selected and all input signals are ignored and all output signals are high impedance. Unless an internal Program, Erase or Write Status Registers embedded operation is in progress, the device will be in the Standby Power mode. Driving the /CS input to logic low state enables the device, placing it in the Active Power mode. After Power Up, a falling edge on /CS is required prior to the start of any instruction.

2.3 Serial Clock (SCLK)

This input signal provides the synchronization reference for the SPI interface. Instructions, addresses, or data input are latched on the rising edge of the SCLK signal. Data output changes after the falling edge of SCLK.

2.4 Serial Input (SI)/IO0

This input signal is used to transfer data serially into the device. It receives instructions, addresses, and data to be programmed. Values are latched on the rising edge of serial SCK clock signal.

SI becomes IO0, an input and output during Dual and Quad Instructions for receiving instructions, addresses, and data to be programmed (values latched on rising edge of serial SCK clock signal) as well as shifting out data (on the falling edge of SCK).

2.5 Serial Data Output (SO)/IO1

This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of the serial SCK clock signal.

SO becomes IO1 an input and output during Dual and Quad Instructions for receiving instructions, addresses, and data to be programmed (values latched on rising edge of serial SCK clock signal) as well as shifting out data (on the falling edge of SCK).

2.6 Write Protect (/WP)/IO2

When /WP is driven Low (VIL), while the Status Register Protect bits (SRP1 and SRP0) of the Status Registers (SR2[0] and SR1[7]) are set to 0 and 1 respectively, it is not possible to write to the Status Registers. This prevents any alteration of the Status Registers. As a consequence, all the data bytes in the memory area that are protected by the Block Protect, TB, SEC bits in the status registers, are also hardware protected against data modification while /WP remains Low. The /WP function is not available when the Quad mode is enabled (QE) in Status Register 2 (SR2[1]=1).

The /WP function is replaced by IO2 for input and output during Quad mode for receiving addresses, and data to be programmed (values are latched on rising edge of the SCK signal) as well as shifting out data (on the falling edge of SCK). /WP has an internal pull-up resistance, when unconnected, /WP is at VIH and may be left unconnected in the host system if not used for Quad mode.

2.7 HOLD (/HOLD)/IO3

The /HOLD signal goes low to stop any serial communications with the device, but doesn't stop the operation of write status register, programming, or erasing in progress.

The operation of HOLD, need /CS keep low, and starts on falling edge of the /HOLD signal, with SCLK signal being low (if SCLK is not being low, HOLD operation will not start until SCLK being low). The HOLD condition ends on rising edge of /HOLD signal with SCLK being low (If SCLK is not being low, HOLD operation will not end until SCLK being low).

When QE=0, the IO3 pin can be configured either as a /HOLD pin or as a /RESET pin depending on Status Register setting. When QE=1, the /HOLD or /RESET function is not available.

2.8 VCC Power Supply

VCC is the supply voltage. It is the single voltage used for all device functions including read, program, and erase.

2.9 VSS Ground

VSS is the reference for the VCC supply voltage.

3. Block/Sector Addresses

Table 2. Block/Sector Addresses of BY25Q64AL

Memory Density	Block(64k byte)	Block(32k byte)	Sector No.	Sector Size(KB)	Address range
64Mbit	Block 0	Half block 0	Sector 0	4	000000h-000FFFh
			:	:	:
			Sector 7	4	007000h-007FFFh
		Half block 1	Sector 8	4	008000h-008FFFh
			:	4	:
			Sector 15	4	00F000h-00FFFFh
	Block 1	Half block 2	Sector 16	4	010000h-010FFFh
			:	:	:
			Sector 23	4	017000h-017FFFh
		Half block 3	Sector 24	4	018000h-018FFFh
			:	:	:
			Sector 31	4	01F000h-01FFFFh
	:	:	:	:	:
	Block 126	Half block 250	Sector 2016	4	7E0000h-7E0FFFh
			:	:	:
			Sector 2023	4	7E7000h-7E7FFFh
		Half block 251	Sector 2024	4	7E8000h-7E8FFFh
			:	:	:
			Sector 2031	4	7EF000h-7EFFFFh
	Block 127	Half block 252	Sector 2032	4	7F0000h-7F0FFFh
			:	:	:
			Sector 2039	4	7F7000h-7F7FFFh
		Half block 253	Sector 2040	4	3F8000h-3F8FFFh
			:	:	:
			Sector 2047	4	7FF000h-7FFFFFh

Notes:
1. Block = Uniform Block, and the size is 64K bytes.
2. Half block = Half Uniform Block, and the size is 32K bytes.
3. Sector = Uniform Sector, and the size is 4K bytes.

4. FUNCTIONAL DESCRIPTIONS

4.1 Standard SPI Instructions

The BY25Q64AL features a serial peripheral interface on 4 signals bus: Serial Clock (SCLK), Chip Select (/CS), Serial Data Input (SI) and Serial Data Output (SO). Both SPI bus mode 0 and 3 are supported. Input data is latched on the rising edge of SCLK and data shifts out on the falling edge of SCLK.

4.2 Dual SPI Instructions

The BY25Q64AL supports Dual SPI operation when using the “Dual Output Fast Read” and “Dual I/O Fast Read” (3Bh and BBh) instructions. These instructions allow data to be transferred to or from the device at two times the rate of the standard SPI. When using the Dual SPI instruction the SI and SO pins become bidirectional I/O pins: IO0 and IO1.

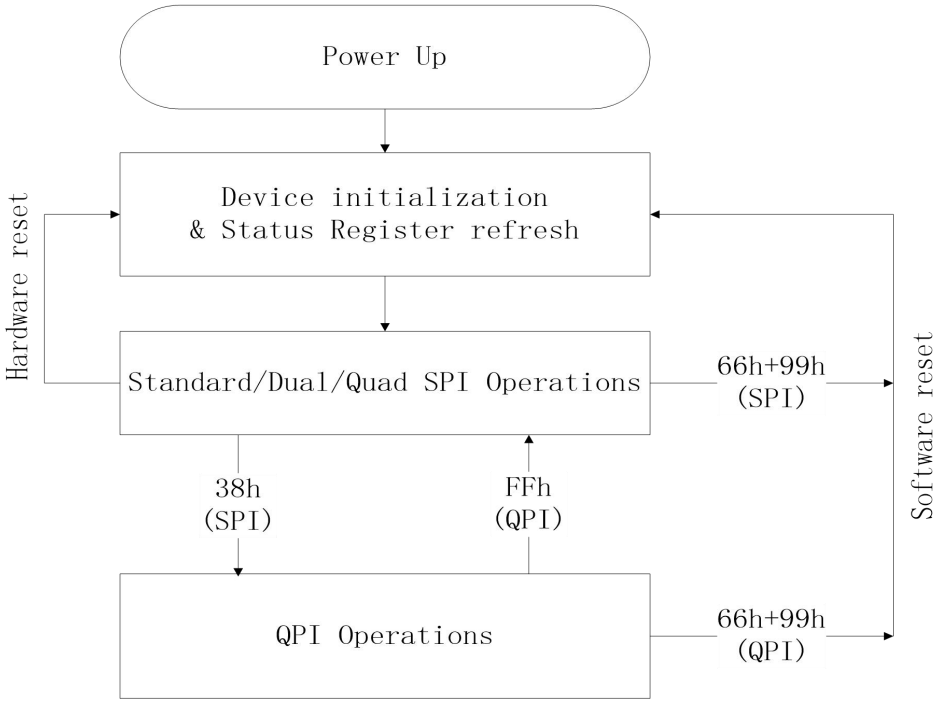
4.3 Quad SPI Instructions

The BY25Q64AL supports Quad SPI operation when using the “Quad Output Fast Read”, “Quad I/O Fast Read”, “Word Read Quad I/O”, “Octal Word Read Quad I/O” (6Bh, EBh, E7h, E3h) instructions. These instructions allow data to be transferred to or from the device at four times the rate of the standard SPI. When using the Quad SPI instruction the SI and SO pins become bidirectional I/O pins: IO0 and IO1, and /WP and /HOLD pins become IO2 and IO3. Quad SPI instructions require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set to 1.

4.4 QPI Instructions

The BY25Q64AL supports Quad Peripheral Interface (QPI) operations only when the device is switched from Standard/Dual/Quad SPI mode to QPI mode using the “Enter QPI (38h)” instruction. The typical SPI protocol requires that the byte-long instruction code being shifted into the device only via DI pin in eight serial clocks. The QPI mode utilizes all four IO pins to input the instruction code, thus only two serial clocks are required. This can significantly reduce the SPI instruction overhead and improve system performance in an XIP environment. Standard/Dual/Quad SPI mode and QPI mode are exclusive. Only one mode can be active at any given time. “Enter QPI (38h)” and “Exit QPI (FFh)” instructions are used to switch between these two modes. Upon power-up or after a software reset using “Enable Reset (66h)” and “Reset (99h)” instruction, the default state of the device is Standard/Dual/Quad SPI mode. To enable QPI mode, the non-volatile Quad Enable bit (QE) in Status Register-2 is required to be set to 1. When using QPI instructions, the DI and DO pins become bidirectional IO0 and IO1, and the /WP and /HOLD pins become IO2 and IO3 respectively.

4.5 Switch between SPI and QPI operation



5. Operation Features

5.1 Supply Voltage

5.1.1 Operating Supply Voltage

Prior to selecting the memory and issuing instructions to it, a valid and stable VCC voltage within the specified [VCC(min), VCC(max)] range must be applied (see *operating ranges*). In order to secure a stable DC supply voltage, it is recommended to decouple the VCC line with a suitable capacitor (usually of the order of 10 *nF* to 100 *nF*) close to the VCC/VSS package pins. This voltage must remain stable and valid until the end of the transmission of the instruction and, for a Write instruction, until the completion of the internal write cycle.

5.1.2 Power-up Conditions

When the power supply is turned on, VCC rises continuously from VSS to VCC. During this time, the Chip Select (/CS) line is not allowed to float but should follow the VCC voltage, it is therefore recommended to connect the /CS line to VCC via a suitable pull-up resistor.

In addition, the Chip Select (/CS) input offers a built-in safety feature, as the /CS input is edge sensitive as well as level sensitive: after power-up, the device does not become selected until a falling edge has first been detected on Chip Select (/CS). This ensures that Chip Select (/CS) must have been High, prior to going Low to start the first operation.

5.1.3 Device Reset

In order to prevent inadvertent Write operations during power-up (continuous rise of VCC), a power on reset (POR) circuit is included. At Power-up, the device does not respond to any instruction until VCC has reached the power on reset threshold voltage (this threshold is lower than the minimum VCC operating voltage defined in *Power-up Timing*).

When VCC is lower than V_{WI}, the device is reset.

5.1.4 Power-down

At Power-down (continuous decrease in VCC), as soon as VCC drops from the normal operating voltage to below the power on reset threshold voltage, the device stops responding to any instruction sent to it. During Power-down, the device must be deselected (Chip Select (/CS) should be allowed to follow the voltage applied on VCC) and in Standby Power mode (that is there should be no internal Write cycle in progress).

5.2 Active Power and Standby Power Modes

When Chip Select (/CS) is Low, the device is selected, and in the Active Power mode. The device consumes ICC.When Chip Select (/CS) is High, the device is deselected. If a Write cycle is not currently in progress, the device then goes in to the Standby Power mode, and the device consumption drops. to ICC1.

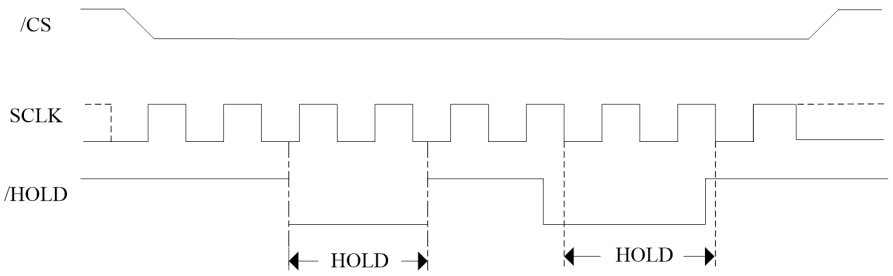
5.3 Hold Condition

The Hold (/HOLD) signal is used to pause any serial communications with the device without resetting the clocking sequence. During the Hold condition, the Serial Data Output (SO) is high impedance, and Serial Data Input (SI) and Serial Clock (SCLK) are Don't Care. To enter the Hold condition, the device must be selected, with Chip Select (/CS) Low. Normally, the device is kept selected, for the whole duration of the Hold condition. Deselecting the device while it is in the Hold condition, has the effect of resetting the state of the device, and this mechanism can be used if it is required to reset any processes that had been in progress.

The Hold condition starts when the Hold (/HOLD) signal is driven Low at the same time as Serial Clock (SCLK) already being Low (as shown in *Figure 5.1*).

The Hold condition ends when the Hold (HOLD) signal is driven High at the same time as Serial Clock (C) already being Low. *Figure 5.1* also shows what happens if the rising and falling edges are not timed to coincide with Serial Clock (SCLK) being Low.

Figure 5.1. Hold condition activation



5.4 Status Register

5.4.1 Status Register Table

See *Table 3*, *Table 4* and *Table 5* for detail description of the Status Register bits. Status Register-3 (SR3), Status Register-2 (SR2) and Status Register-1 (SR1) can be used to provide status on the availability of the Flash memory array: whether the device is write enabled or disabled, the state of write protection, Quad SPI setting, Security Register lock status, and Erase/Program Suspend status, output driver strength, and so on.

Table 3. Status Register-3 (SR3)

BIT	Name	Function	Default Value	Description
7	HOLD / RST	/HOLD or /RESET Function	0	0 = the pin acts as /HOLD 1 = the pin acts as /RESET (Volatile / Non-Volatile, Writable)
6	DRV1	Output Driver Strength	1	determine the output driver strength for the Read operations (See *Table 6* for driver strength) (Volatile / Non-Volatile, Writable)
5	DRV0		0	
4	(R)	Reserved	/	/
3	(R)	Reserved	/	/
2	WPS	Write Protect Selection	0	0 = Write Protect by CMP, SEC, TB, BP[2:0] 1 = Write Protect by the Individual Block Locks (Volatile / Non-Volatile, Writable)
1	(R)	Reserved	/	/
0	(R)	Reserved	/	/

Table 4. Status Register-2 (SR2)

BIT	Name	Function	Default Value	Description
7	SUS1	Suspend Status	0	0 = Erase not suspended 1 = Erase suspended (Volatile, Read-Only)
6	CMP	Complement Protect	0	0 = Normal Protection Map 1 = Inverted Protection Map (Volatile / Non-Volatile, Writable)
5	LB3	Security Register Lock Bits	0	OTP Lock Bits 3:1 for Security Registers 3:1 0 = Security Register not protected 1 = Security Register protected (Volatile / Non-Volatile, OTP Writable)
4	LB2		0	
3	LB1		0	
2	SUS2	Suspend Status	0	0 = Program not suspended 1 = Program suspended (Volatile, Read-Only)
1	QE	Quad Enable	0	0 = Quad Mode Not Enabled, the /WP and /HOLD pins are enabled. 1 = Quad Mode Enabled, the IO2 and IO3 pins are enabled, and /WP and /HOLD functions are disabled (Volatile / Non-Volatile, Writable)
0	SRP1	Status Resister Protect 1	0	0 = SRP0 selects whether /WP input has effect on protection of the status register 1 = SRP0 selects Power Supply Lock Down or OTP Lock Down mode (Volatile / Non-Volatile, Writable)

Table 5. Status Register-1 (SR1)

BIT	Name	Function	Default Value	Description
7	SRP0	Status Resister Protect 0	0	0 = /WP input has no effect or Power Supply Lock Down mode 1 = /WP input can protect the Status Register or OTP Lock Down (Volatile / Non-Volatile, Writable)
6	SEC	Sector/Block Protect	0	0 = BP2-BP0 protect 64KB blocks 1 = BP2-BP0 protect 4KB sectors (Volatile / Non-Volatile, Writable)
5	TB	Top/Bottom Protect	0	0 = BP2-BP0 protect from the Top down 1 = BP2-BP0 protect from the Bottom up (Volatile / Non-Volatile, Writable)
4	BP2	Block Protect Bits	0	000b = No protection See *Table 8* and *Table 9* for protection ranges (Volatile / Non-Volatile, Writable)
3	BP1		0	
2	BP0		0	
1	WEL	Write Enable Latch	0	0 = Not Write Enabled, no embedded operation can start 1 = Write Enabled, embedded operation can start (Volatile, Read-Only)
0	WIP	Write in Progress Status	0	0 = Not Busy, no embedded operation in progress 1 = Busy, embedded operation in progress (Volatile, Read-Only)

5.4.2 The Status and Control Bits

5.4.2.1 WIP bit

The Write in Progress (WIP) bit indicates whether the memory is busy in program / erase / write status register progress. When WIP bit is set to 1, means that the device is busy in program / erase / write status register progress, when WIP bit is cleared to 0, means that the device is not in program / erase / write status register progress.

5.4.2.2 WEL bit

The Write Enable Latch bit indicates the status of the internal Write Enable Latch. When WEL bit is set to 1 the internal Write Enable Latch is set, when WEL bit is cleared to 0 the internal Write Enable Latch is reset and no Write Status Register, Program or Erase instruction is accepted.

5.4.2.3 SEC, TB, BP2, BP1, BP0 bits

The Block Protect (SEC, TB, BP2, BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase instructions. These bits are written with the Write Status Register instruction. When the Block Protect (SEC, TB, BP2, BP1, BP0) bits are set to 1, the relevant memory (as defined in *Table 8* and *Table 9*) are became protected against Page Program, Sector Erase and Block Erase instructions. The Block Protect (SEC, TB, BP2, BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set.

5.4.2.4 SRP1, SRP0 bits

The Status Register Protect (SRP1 and SRP0) bits are non-volatile Read/Write bits in the status register. The SRP bits control the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable protection.

5.4.2.5 QE bit

The Quad Enable (QE) bit is a non-volatile Read/Write bit in the Status Register that allows Quad SPI and QPI operation. When the QE bit is set to 0 (Default) the /WP pin and /HOLD pin are enable. When the QE pin is set to 1, the Quad IO2 and IO3 pins are enabled. (The QE bit should never be set to 1 during standard SPI or Dual SPI operation if the /WP or /HOLD pins directly to the power supply).

QE bit is required to be set to 1 before issuing an “Enter QPI (38h)” instruction to switch the device from Standard/Dual/Quad SPI mode to QPI mode; otherwise the command (38h) will be ignored. When the device is in QPI mode, QE bit will remain to be 1. A “Write Status Register” command in QPI mode cannot change QE bit from 1 to 0.

5.4.2.6 LB3/LB2/LB1 bit

The LB bit is a non-volatile One Time Program (OTP) bit in Status Register that provide the write protect control and status to the Security Registers. The default state of LB is 0, the security registers are unlocked. LB can be set to 1 individually using the Write Register instruction. LB is One Time Programmable, once it’s set to 1, the 256byte Security Registers will become read-only permanently, LB3/2/1 for Security Registers 3:1.

5.4.2.7 SUS bit

The Suspend Status (SUS1 and SUS2) bits are read only bits in the status register2 (S15 and S10) that are set to 1 after executing a Erase/Program Suspend (75H) instruction (The Erase Suspend will set SUS1 to 1, and the Program Suspend will set the SUS2 to 1). The SUS1 and SUS2 bits are cleared to 0 by Erase/Program Resume (7AH) instruction as well as a power-down, power-up cycle.

5.4.2.8 Complement Protect (CMP)

The Complement Protect bit (CMP) is a non-volatile read/write bit in the status register. It is used in conjunction with SEC, TB, BP2, BP1 and BP0 bits to provide more flexibility for the array protection. Once CMP is set to 1, previous array protection set by SEC, TB, BP2, BP1 and BP0 will be reversed. For instance, when CMP=0, a top 64KB block can be protected while the rest of the array is not; when CMP=1, the top 64KB block will become unprotected while the rest of the array become read-only. Please refer to the *Status Register Memory Protection table* for details. The default setting is CMP=0.

5.4.2.9 Write Protect Selection (WPS)

The WPS bit is used to select which Write Protect scheme should be used. When WPS=0, the device will use the combination of CMP, SEC, TB, BP[2:0] bits to protect a specific area of the memory array. When WPS=1, the device will utilize the Individual Block Locks to protect any individual sector or blocks. The default value for all Individual Block Lock bits is 1 upon device power on or after reset.

5.4.2.10 Output Driver Strength (DRV1, DRV0)

The DRV1 & DRV0 bits are used to determine the output driver strength for the Read operations.

Table 6. Output driver strength table

DRV1,DRV0	Driver Strength
0,0	100%
0,1	75%
1,0	50%
1,1	25%

5.4.2.11 /HOLD or /RESET Pin Function (HOLD/RST)

The HOLD/RST bit is used to determine whether /HOLD or /RESET function should be implemented on the hardware pin for 8- pin packages. When HOLD/RST=0 (factory default), the pin acts as /HOLD; when HOLD/RST=1, the pin acts as /RESET. However, /HOLD or /RESET functions are only available when QE=0. If QE is set to 1, the /HOLD and /RESET functions are disabled, the pin acts as a dedicated data I/O pin.

5.4.2.12 Reserved Bits – Non Functional

There are a few reserved Status Register bits that may be read out as a “0” or “1”. It is recommended to ignore the values of those bits. During a “Write Status Register” instruction, the Reserved Bits can be written as “0”, but there will not be any effects

5.4.3 Status Register Protect Table

Table 7. Status Register protect table

SRP1	SRP0	/WP	Status Register	Description
0	0	X	Software Protected	The Status Register can be written to after a Write Enable instruction, WEL=1.(Factory Default)
0	1	0	Hardware Protected	/WP=0, the Status Register locked and cannot be written.
0	1	1	Hardware Unprotected	/WP=1, the Status Register is unlocked and can be written to after a Write Enable instruction, WEL=1.
1	0	X	Power Supply Lock-Down(1)	Status Register is protected and cannot be written to again until the next Power-Down, Power-Up cycle.
1	1	X	One Time Program(2)	Status Register is permanently protected and cannot be written to.

Notes:
1. When SRP1, SRP0= (1, 0), a Power-Down, Power-Up cycle will change SRP1, SRP0 to (0, 0) state.
2. The One time Program feature is available upon special order. Please contact BY Technology for details.

5.4.4 Write Protect Features

1. Software Protection: The Block Protect (SEC, TB, BP2, BP1, BP0) bits define the section of the memory array that can be read but not change.
2. Hardware Protection: /WP going low to protected the BP0~SEC bits and SRP0~1 bits.
3. Deep Power-Down: In Deep Power-Down Mode, all instructions are ignored except the Release from deep Power-Down Mode instruction.
4. Write Enable: The Write Enable Latch (WEL) bit must be set prior to every Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register and Erase/Program Security Registers instruction.

5.4.5 Status Register Memory Protection

5.4.5.1 Protect Table (WPS=0)

Table 8. BY25Q64AL Status Register Memory Protection (WPS = 0, CMP = 0)

Status Register Content					Memory Content			
BP4	BP3	BP2	BP1	BP0	Blocks	Addresses	Density	Portion
X	X	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	126 to 127	7E0000H-7FFFFFH	128KB	Upper 1/64
0	0	0	1	0	124 to 127	7C0000H-7FFFFFH	256KB	Upper 1/32
0	0	0	1	1	120 to 127	780000H-7FFFFFH	512KB	Upper 1/16
0	0	1	0	0	112 to 127	700000H-7FFFFFH	1MB	Upper 1/8
0	0	1	0	1	96 to 127	600000H-7FFFFFH	2MB	Upper 1/4
0	0	1	1	0	64 to 127	400000H-7FFFFFH	4MB	Upper 1/2
0	1	0	0	1	0 to 1	000000H-01FFFFH	128KB	Lower 1/64
0	1	0	1	0	0 to 3	000000H-03FFFFH	256KB	Lower 1/32
0	1	0	1	1	0 to 7	000000H-07FFFFH	512KB	Lower 1/16
0	1	1	0	0	0 to 15	000000H-0FFFFFH	1MB	Lower 1/8
0	1	1	0	1	0 to 31	000000H-1FFFFFH	2MB	Lower 1/4
0	1	1	1	0	0 to 63	000000H-3FFFFFH	4MB	Lower 1/2
X	X	1	1	1	0 to 127	000000H-7FFFFFH	8MB	ALL
1	0	0	0	1	127	7FF000H-7FFFFFH	4KB	Top Block
1	0	0	1	0	127	7FE000H-7FFFFFH	8KB	Top Block
1	0	0	1	1	127	7FC000H-7FFFFFH	16KB	Top Block
1	0	1	0	X	127	7F8000H-7FFFFFH	32KB	Top Block
1	0	1	1	0	127	7F8000H-7FFFFFH	32KB	Top Block
1	1	0	0	1	0	000000H-000FFFH	4KB	Bottom Block
1	1	0	1	0	0	000000H-001FFFH	8KB	Bottom Block
1	1	0	1	1	0	000000H-003FFFH	16KB	Bottom Block
1	1	1	0	X	0	000000H-007FFFH	32KB	Bottom Block
1	1	1	1	0	0	000000H-007FFFH	32KB	Bottom Block

Notes:

1. X = don't care
2. L = Lower; U = Upper
3. If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored.

Table 9. Status Register Memory Protection (WPS = 0, CMP = 1)

Status Register Content					Memory Content			
BP4	BP3	BP2	BP1	BP0	Blocks	Addresses	Density	Portion
X	X	0	0	0	ALL	000000H-7FFFFFH	ALL	ALL
0	0	0	0	1	0 to 125	000000H-7DFFFFH	8064KB	Lower 63/64
0	0	0	1	0	0 to 123	000000H-7BFFFFH	7936KB	Lower 31/32
0	0	0	1	1	0 to 119	000000H-77FFFFH	7680KB	Lower 15/16
0	0	1	0	0	0 to 111	000000H-6FFFFFH	7MB	Lower 7/8
0	0	1	0	1	0 to 95	000000H-5FFFFFH	6MB	Lower 3/4
0	0	1	1	0	0 to 63	000000H-3FFFFFH	4MB	Lower 1/2
0	1	0	0	1	2 to 127	020000H-7FFFFFH	8064KB	Upper 63/64
0	1	0	1	0	4 to 127	040000H-7FFFFFH	7936KB	Upper 31/32
0	1	0	1	1	8 to 127	080000H-7FFFFFH	7680KB	Upper 15/16
0	1	1	0	0	16 to 127	100000H-7FFFFFH	7MB	Upper 7/8
0	1	1	0	1	32 to 127	200000H-7FFFFFH	6MB	Upper 3/4
0	1	1	1	0	64 to 127	400000H-7FFFFFH	4MB	Upper 1/2
X	X	1	1	1	NONE	NONE	NONE	NONE
1	0	0	0	1	0 to127	000000H-7FEFFFH	8188KB	L-2047/2048
1	0	0	1	0	0 to 127	000000H-7FDFFFH	8184KB	L-1023/1024
1	0	0	1	1	0 to 127	000000H-7FBFFFH	8176KB	L-511/512
1	0	1	0	X	0 to 127	000000H-7F7FFFH	8160KB	L-255/256
1	0	1	1	0	0 to 127	000000H-7F7FFFH	8160KB	L-255/256
1	1	0	0	1	0 to127	001000H-7FFFFFH	8188KB	U-2047/2048
1	1	0	1	0	0 to 127	002000H-7FFFFFH	8184KB	U-1023/1024
1	1	0	1	1	0 to 127	004000H-7FFFFFH	8176KB	U-511/512
1	1	1	0	X	0 to 127	008000H-7FFFFFH	8160KB	U-255/256
1	1	1	1	0	0 to 127	008000H-7FFFFFH	8160KB	U-255/256

Notes:

1. X = don’t care
2. L = Lower; U = Upper
3. If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored.

5.4.5.2 Dynamic Protection Bits (WPS=1)

The Dynamic Protection Bits (DPBs) are volatile bits for quickly and easily enabling or disabling write-protection to sectors and blocks. A DPB is assigned to each 4KB sector in the bottom and top 64KB of memory and to each 64KB block in the rest of the memory.

When a DPB is “1”, the associated sector or block will be write-protected, preventing any program or erase operation on the sector or block. All DPBs default to “1” after power-on or reset. When a DPB is cleared to “0”, the associated sector or block will be unprotected if the corresponding SPB is also “0”.

DPB bits can be individually set to “1” or “0” by the Dynamic Protection Block/Sector Lock/Dynamic Protection Block/Sector Unlock instruction. The DBP bits can also be globally cleared to “0” with the Global Block/Sector Unlock instruction or globally set to “1” with the Global Block/Sector Lock instruction. A Write Enable instruction must be executed to set the WEL bit before sending the Dynamic Protection Block/Sector Lock, Dynamic Protection Block/Sector Unlock, Global Block/Sector Lock, or Global Block/Sector Unlock instruction.

The Read Block/Sector Lock instruction reads the status of the DPB of a sector or block. The Read Block/Sector Lock instruction returns 00h if the DPB is “0”, indicating write-protection is disabled. The Read Block/Sector Lock instruction returns 01h if the DPB is “1”, indicating write-protection is enabled.

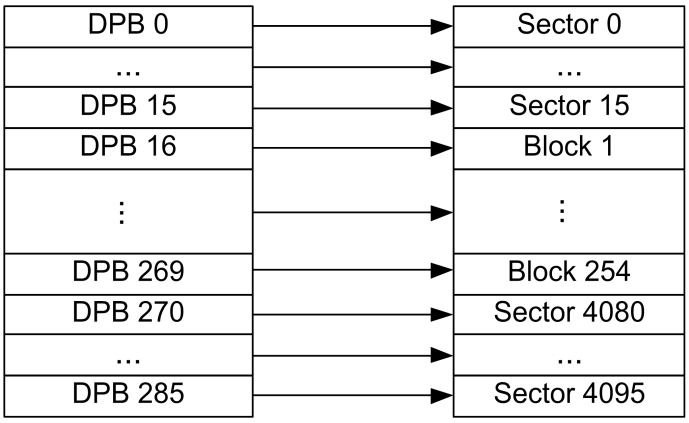


Table Dynamic Protection Bit

Description	Bit Status	Default	Type
Dynamic Protection Bit (DPB)	0 = Unprotect Sector / Block 1 = Protect Sector / Block	1	Volatile

6. Device Identification

Three legacy Instructions (9Fh/90h/ABh) and 2 new instructions(92h/94h) in Dual/Quad SPI mode are supported to access device identification that can indicate the manufacturer, device type, and capacity (density). The returned data bytes provide the information as shown in the below table.

Table 10. BY25Q64AL ID Definition table

Operation Code	M7-M0	ID15-ID8	ID7-ID0
9Fh	68	60	17
90h / 92h /94h	68		16
ABh			16

7. Instructions Description

All instructions, addresses and data are shifted in and out of the device, beginning with the most significant bit on the first rising edge of SCLK after /CS is driven low. Then, the one byte instruction code must be shifted in to the device, most significant bit first on SI, each bit being latched on the rising edges of SCLK.

See *Table 11/12/13*, every instruction sequence starts with a one-byte instruction code. Depending on the instruction, this might be followed by address bytes, or by data bytes, or by both or none. /CS must be driven high after the last bit of the instruction sequence has been shifted in. For the instruction of Read, Fast Read, Read Status Register or Release from Deep Power Down, and Read Device ID, the shifted-in instruction sequence is followed by a data out sequence. /CS can be driven high after any bit of the data-out sequence is being shifted out.

For the instruction of Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Write Enable, Write Disable or Deep Power-Down instruction, /CS must be driven high exactly at a byte boundary, otherwise the instruction is rejected, and is not executed. That is /CS must drive high when the number of clock pulses after /CS being driven low is an exact multiple of eight. For Page Program, if at any time the input byte is not a full byte, nothing will happen and WEL will not be reset.

Table 11. Instruction Set Table 1 (Standard/Dual/Quad SPI Instructions)(1)

Instruction Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6
Write Enable	06h					
Volatile SR Write Enable	50h					
Write Disable	04h					
Read Status Register-1	05h	(S7-S0)(2)				
Write Status Register-1(4)	01h	(S7-S0)(4)				
Read Status Register-2	35h	(S15-S8)(2)				
Write Status Register-2	31h	(S15-S8)				
Read Status Register-3	15h	(S23-S16)(2)				
Write Status Register-3	11h	(S23-S16)				
Chip Erase	C7h/60h					
Erase/Program Suspend	75h					
Erase/Program Resume	7Ah					
Power-down	B9h					
Release Power-down / ID	ABh	Dummy	Dummy	Dummy	(ID7-ID0)(2)	
Manufacturer/Device ID	90h	Dummy	Dummy	00h	(MF7-MF0)	(ID7-ID0)(2)
JEDEC ID	9Fh	(MF7-MF0)	(ID15-ID8)	(ID7-ID0)(2)		
Global Block Lock	7Eh					
Global Block Unlock	98h					
Enter QPI Mode	38h					
Enable Reset	66h					
Reset Device	99h					
Read Serial Flash Discoverable Parameter	5Ah	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	Next bytes
Instruction Name	**Byte 1**	**Byte 2**	**Byte 3**	**Byte 4**	**Byte 5**	**Byte 6 ~ Byte 21**
Read Unique ID	4Bh	Dummy	Dummy	Dummy	Dummy	(UID127-UID0)

Table 12. Instruction Set Table 2 (Standard/Dual/Quad SPI Instructions) (1)

Instruction Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8	Byte 9
Page Program	02h	A23-A16	A15-A8	A7-A0	D7-D0(3)	Next bytes			
Quad Page Program	32h	A23-A16	A15-A8	A7-A0	D7-D0(3)(9)	Next bytes			
Sector Erase (4KB)	20h	A23-A16	A15-A8	A7-A0					
Block Erase (32KB)	52h	A23-A16	A15-A8	A7-A0					
Block Erase (64KB)	D8h	A23-A16	A15-A8	A7-A0					
Read Data	03h	A23-A16	A15-A8	A7-A0	(D7-D0)	(D7-D0)	Next bytes		
Fast Read	0Bh	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	Next bytes		
Fast Read Dual Output	3Bh	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)(7)	Next bytes		
Fast Read Quad Output	6Bh	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)(9)	Next bytes		
Erase Security Register(5)	44h	A23-A16	A15-A8	A7-A0					
Program Security Register(5)	42h	A23-A16	A15-A8	A7-A0	D7-D0(3)	Next bytes			
Read Security Register(5)	48h	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	Next bytes		
Dynamic Protection Block/Sector Lock	36h	A23-A16	A15-A8	A7-A0					
Dynamic Protection Block/Sector Unlock	39h	A23-A16	A15-A8	A7-A0					
Read Block/Sector Lock	3Dh	A23-A16	A15-A8	A7-A0	(L7-L0)				
Fast Read Dual I/O	BBh	A23-A16(6)	A15-A8(6)	A7-A0(6)	M7-M0(6)	(D7-D0)(7)			
Mftr./Device ID Dual I/O	92h	A23-A16(6)	A15-A8(6)	A7-A0(6)	M7-M0(6)	(MF7-MF0)(7)	(D7-D0)(7)		
Set Burst with Wrap	77h	Dummy	Dummy	Dummy	W8-W0				
Fast Read Quad I/O(10)	EBh	A23-A16(8)	A15-A8(8)	A7-A0(8)	M7-M0(8)	Dummy	Dummy	(D7-D0)(9)	Next byte
Word Read Quad I/O(11) (12)	E7h	A23-A16(8)	A15-A8(8)	A7-A0(8)	M7-M0(8)	Dummy	(D7-D0)(9)	Next bytes	
Octal Word Read Quad I/O(13)	E3h	A23-A16(8)	A15-A8(8)	A7-A0(8)	M7-M0(8)	(D7-D0)(9)	Next bytes		
Mftr./Device ID Quad I/O	94h	A23-A16(8)	A15-A8(8)	A7-A0(8)	M7-M0(8)	Dummy	Dummy	(MF7-MF0)(9)	(ID7-ID0)(9)

Table 13. Instruction Set Table 3 (QPI Instructions) (14)

Instruction Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6
Write Enable	06h					
Volatile SR Write Enable	50h					
Write Disable	04h					
Read Status Register-1	05h	(S7-S0)(2)				
Write Status Register-1(4)	01h	(S7-S0)(4)				
Read Status Register-2	35h	(S15-S8)(2)				
Write Status Register-2	31h	(S15-S8)				
Read Status Register-3	15h	(S23-S16)(2)				
Write Status Register-3	11h	(S23-S16)				
Chip Erase	C7h/60h					
Erase/Program Suspend	75h					
Erase/Program Resume	7Ah					
Power-down	B9h					
Set Read Parameters	C0h	P7-P0				
Release Powerdown / ID	ABh	Dummy	Dummy	Dummy	(ID7-ID0)(2)	
Manufacturer/Device ID	90h	Dummy	Dummy	00h	(MF7-MF0)(2)	(ID7-ID0)(2)
JEDEC ID	9Fh	(MF7-MF0)(2)	(ID15-ID8)(2)	(ID7-ID0)(2)		
Global Block Lock	7Eh					
Global Block Unlock	98h					
Exit QPI Mode	FFh					
Enable Reset	66h					
Reset Device	99h					
Page Program	02h	A23-A16	A15-A8	A7-A0	D7-D0(3)(9)	Next bytes
Sector Erase (4KB)	20h	A23-A16	A15-A8	A7-A0		
Block Erase (32KB)	52h	A23-A16	A15-A8	A7-A0		
Block Erase (64KB)	D8h	A23-A16	A15-A8	A7-A0		
Fast Read	0Bh	A23-A16	A15-A8	A7-A0	Dummy(15)	(D7-D0)
Burst Read with Wrap(16)	0Ch	A23-A16	A15-A8	A7-A0	Dummy(15)	(D7-D0)
Fast Read Quad I/O	EBh	A23-A16	A15-A8	A7-A0	M7-M0(15)	(D7-D0)
Dynamic Protection Block/Sector Lock	36h	A23-A16	A15-A8	A7-A0		
Dynamic Protection Block/Sector Unlock	39h	A23-A16	A15-A8	A7-A0		
Read Block/Sector Lock	3Dh	A23-A16	A15-A8	A7-A0	(L7-L0)	
Read Serial Flash Discoverable Parameter	5Ah	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)

Notes:

1. Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis “( )” indicate data output from the device on 1, 2 or 4 IO pins.
2. The Status Register contents and Device ID will repeat continuously until /CS terminates the instruction.
3. At least one byte of data input is required for Page Program, Quad Page Program and Program Security Registers, up to 256 bytes of data input. If more than 256 bytes of data are sent to the device, the addressing will wrap to the beginning of the page and overwrite previously sent data.
4. Write Status Register-1 (01h) can also be used to program Status Register-1&2, see *section 7.1.5*.

5. Security Register Address:

Security Register 1	A23-16 = 00h	A15-8 = 10h	A7-0 = byte address
Security Register 2	A23-16 = 00h	A15-8 = 20h	A7-0 = byte address
Security Register 3	A23-16 = 00h	A15-8 = 30h	A7-0 = byte address

6. Dual SPI address input format:
   IO0 = A22, A20, A18, A16, A14, A12, A10, A8, A6, A4, A2, A0, M6, M4, M2, M0
   IO1 = A23, A21, A19, A17, A15, A13, A11, A9, A7, A5, A3, A1, M7, M5, M3, M1
7. Dual SPI data output format:
   IO0 = (D6, D4, D2, D0)
   IO1 = (D7, D5, D3, D1)
8. Quad SPI address input format:
   IO0 = A20, A16, A12, A8, A4, A0, M4, M0
   IO1 = A21, A17, A13, A9, A5, A1, M5, M1
   IO2 = A22, A18, A14, A10, A6, A2, M6, M2
   IO3 = A23, A19, A15, A11, A7, A3, M7, M3
9. Quad SPI data input/output format:
   IO0 = (D4, D0, …..)
   IO1 = (D5, D1, …..)
   IO2 = (D6, D2, …..)
   IO3 = (D7, D3, …..)
10. Fast Read Quad I/O data output format:
    IO0 = (x, x, x, x, D4, D0, D4, D0)
    IO1 = (x, x, x, x, D5, D1, D5, D1)
    IO2 = (x, x, x, x, D6, D2, D6, D2)
    IO3 = (x, x, x, x, D7, D3, D7, D3)
11. Word Read Quad I/O data output format:
    IO0 = (x, x, D4, D0, D4, D0, D4, D0)
    IO1 = (x, x, D5, D1, D5, D1, D5, D1)
    IO2 = (x, x, D6, D2, D6, D2, D6, D2)
    IO3 = (x, x, D7, D3, D7, D3, D7, D3)
12. For Word Read Quad I/O, the lowest address bit must be 0. (A0 = 0)
13. For Octal Word Read Quad I/O, the lowest four address bits must be 0. (A3, A2, A1, A0 = 0)
14. QPI Command, Address, Data input/output format:

CLK # 0 1	*2 3*	*4 5*	*6 7*	*8 9*	*10 11*
IO0 = C4, C0,	A20, A16,	A12, A8,	A4, A0,	D4, D0,	D4, D0
IO1 = C5, C1,	A21, A17,	A13, A9,	A5, A1,	D5, D1,	D5, D1
IO2 = C6, C2,	A22, A18,	A14, A10,	A6, A2,	D6, D2,	D6, D2
IO3 = C7, C3,	A23, A19,	A15, A11,	A7, A3,	D7, D3,	D7, D3

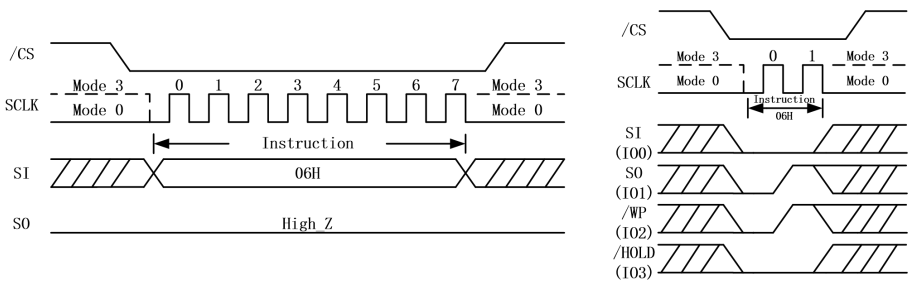
15. The number of dummy clocks for QPI Fast Read, QPI Fast Read Quad I/O & QPI Burst Read with Wrap is controlled by read parameter P7 – P4.
16. The wrap around length for QPI Burst Read with Wrap is controlled by read parameter P3 – P0.

7.1 Configuration and Status Instructions

7.1.1 Write Enable (06H)

The Write Enable instruction (*Figure 7.1.1*) sets the Write Enable Latch (WEL) bit in the Status Register to a 1. The WEL bit must be set prior to every Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register and Erase/Program Security Registers instruction. The Write Enable instruction is entered by driving /CS low, shifting the instruction code “06h” into the Serial Input (SI) pin on the rising edge of SCLK, and then driving /CS high.

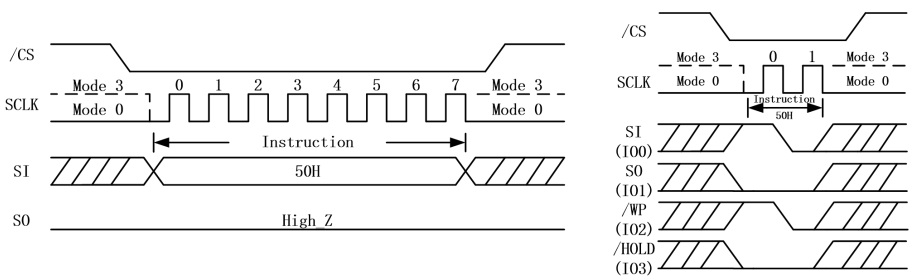
Figure 7.1.1. Write Enable Instruction for SPI Mode (left) or QPI Mode (right)



7.1.2 Write Enable for Volatile Status Register (50h)

The non-volatile Status Register bits described in *section 5.4* can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. To write the volatile values into the Status Register bits, the Write Enable for Volatile Status Register (50h) instruction must be issued prior to a Write Status Register (01h) instruction. Write Enable for Volatile Status Register instruction (*Figure 7.1.2*) will not set the Write Enable Latch (WEL) bit, it is only valid for the Write Status Register instruction to change the volatile Status Register bit values.

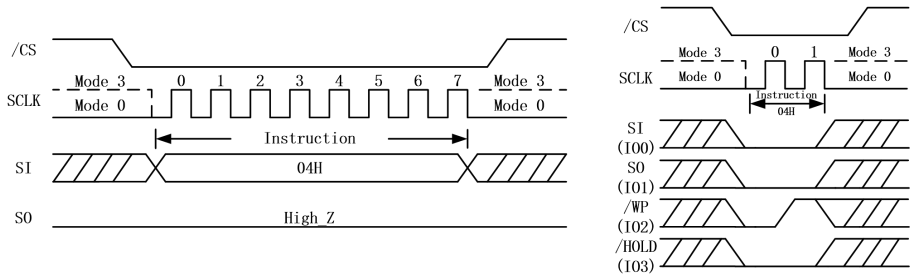
Figure 7.1.2. Write Enable for Volatile Status Register Instruction for SPI Mode (left) or QPI Mode (right)



7.1.3 Write Disable (04h)

The Write Disable instruction (*Figure 7.1.3*) resets the Write Enable Latch (WEL) bit in the Status Register to 0. The Write Disable instruction is entered by driving /CS low, shifting the instruction code “04h” into the SI pin and then driving /CS high. Note that the WEL bit is automatically reset after Power-up and upon completion of the Write Status Register, Erase/Program Security Registers, Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase and Reset instructions.

Figure 7.1.3. Write Disable Instruction for SPI Mode (left) or QPI Mode (right)



7.1.4 Read Status Register-1 (05h), Status Register-2 (35h) & Status Register-3 (15h)

The Read Status Register instructions allow the 8-bit Status Registers to be read. The instruction is entered by driving /CS low and shifting the instruction code “05h” for Status Register-1, “35h” for Status Register -2 or “15h” for Status Register-3 into the SI pin on the rising edge of SCLK. The status register bits are then shifted out on the SO pin at the falling edge of SCLK with most significant bit (MSB) first as shown in Figure *7.1.4a*(SPI mode) and Figure *7.1.4b*(QPI mode). Refer to *section 5.4* for Status Register descriptions.

The Read Status Register instruction may be used at any time, even while a Program, Erase or Write Status Register cycle is in progress. This allows the BUSY status bit to be checked to determine when the cycle is complete and if the device can accept another instruction. The Status Register can be read continuously, as shown in Figure *7.1.4a*(SPI mode) and Figure *7.1.4b*(QPI mode). The instruction is completed by driving /CS high.

Figure 7.1.4a. Read Status Register Instruction (SPI Mode)

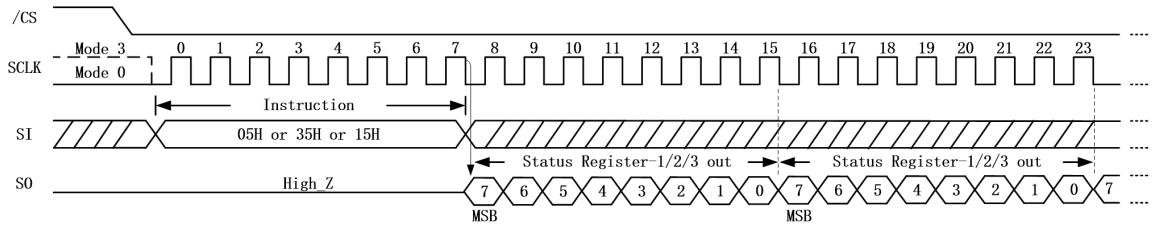
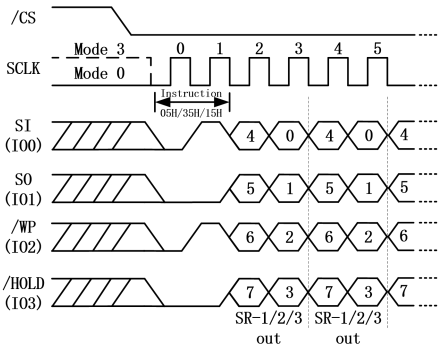


Figure 7.1.4b. Read Status Register Instruction (QPI Mode)



7.1.5 Write Status Register-1 (01h), Status Register-2 (31h) & Status Register-3 (11h)

The Write Status Register instruction allows the Status Registers to be written. The writable Status Register bits include: SRP0, SEC, TB, BP[2:0] in Status Register-1; CMP, LB[3:1], QE, SRP1 in Status Register- 2; HOLD/RST, DRV1, DRV0, WPS in Status Register-3. All other Status Register bit locations are read-only and will not be affected by the Write Status Register instruction. LB[3:1] are non-volatile OTP bits, once it is set to 1, it cannot be cleared to 0.

To write non-volatile Status Register bits, a standard Write Enable (06h) instruction must previously have been executed for the device to accept the Write Status Register instruction (Status Register bit WEL must equal 1). Once write enabled, the instruction is entered by driving /CS low, sending the instruction code “01h/31h/11h”, and then writing the status register data byte as illustrated in *Figure 7.1.5a*(SPI mode) & *Figure 7.1.5b*(QPI mode).

To write volatile Status Register bits, a Write Enable for Volatile Status Register (50h) instruction must have been executed prior to the Write Status Register instruction (Status Register bit WEL remains 0). However, SRP1 and LB[3:1] cannot be changed from “1” to “0” because of the OTP protection for these bits. Upon power off or the execution of a Software/Hardware Reset, the volatile Status Register bit values will be lost, and the non-volatile Status Register bit values will be restored.

During non-volatile Status Register write operation (06h combined with 01h/31h/11h), after /CS is driven high, the self-timed Write Status Register cycle will commence for a time duration of tW (See *AC Characteristics*). While the Write Status Register cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Write Status Register cycle and a 0 when the cycle is finished and ready to accept other instructions again. After the Write Status Register cycle has finished, the Write Enable Latch (WEL) bit in the Status Register will be cleared to 0.

During volatile Status Register write operation (50h combined with 01h/31h/11h), after /CS is driven high, the Status Register bits will be refreshed to the new values within the time period of tSHSL2 (See *AC Characteristics*). BUSY bit will remain 0 during the Status Register bit refresh period.

The Write Status Register instruction can be used in both SPI mode and QPI mode. However, the QE bit cannot be written to when the device is in the QPI mode, because QE=1 is required for the device to enter and operate in the QPI mode.

Refer to *section 5.4* for Status Register descriptions. Factory default for all status Register bits are 0.

Figure 7.1.5a. Write Status Register-1/2/3 Instruction (SPI Mode)

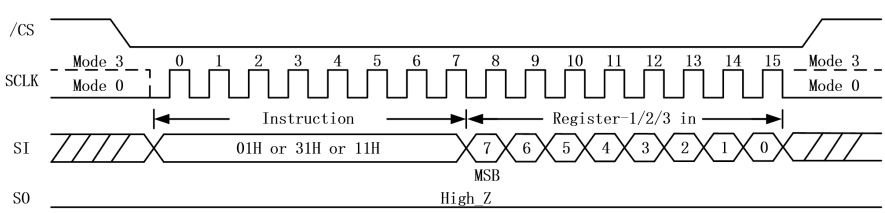
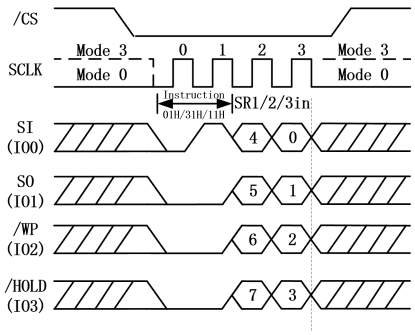


Figure 7.1.5b. Write Status Register-1/2/3 Instruction (QPI Mode)



The BY25Q64AL is also backward compatible to BY Technology's previous generations of serial flash memories, in which the Status Register-1&2 can be written using a single "Write Status Register-1 (01h)" command. To complete the Write Status Register- 1&2 instruction, the /CS pin must be driven high after the sixteenth bit of data that is clocked in as shown in *Figure 7.1.5c*(SPI mode) & *Figure 7.1.5d*(QPI mode). If /CS is driven high after the eighth clock, the Write Status Register-1 (01h) instruction will only program the Status Register-1, the Status Register-2 will not be affected (Previous generations will clear CMP and QE bits).

Figure 7.1.5c. Write Status Register-1/2 Instruction (SPI Mode)

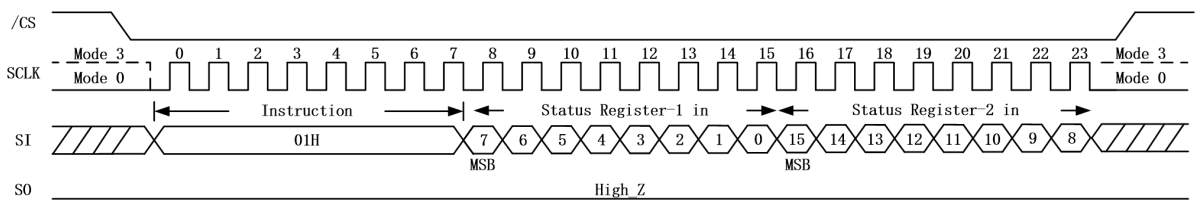
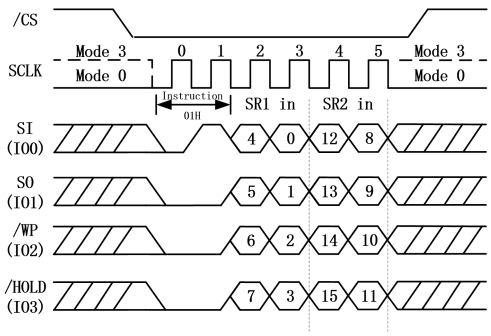


Figure 7.1.5d. Write Status Register-1/2 Instruction (QPI Mode)



7.2 Read Instructions

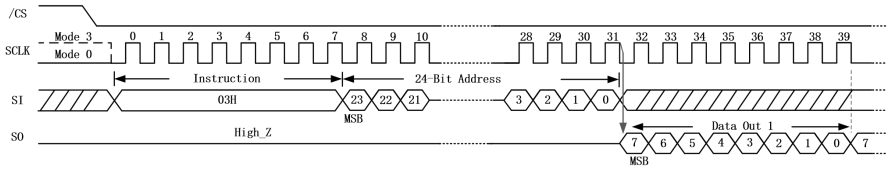
7.2.1 Read Data (03H)

The Read Data instruction allows one or more data bytes to be sequentially read from the memory. The instruction is initiated by driving the /CS pin low and then shifting the instruction code “03h” followed by a 24-bit address (A23-A0) into the SI pin. The code and address bits are latched on the rising edge of the SCLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the SO pin at the falling edge of SCLK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. This means that the entire memory can be accessed with a single instruction as long as the clock continues. The instruction is completed by driving /CS high.

The Read Data instruction sequence is shown in *Figure 7.2.1*. If a Read Data instruction is issued while an Erase, Program or other Write cycle is in process (BUSY=1) the instruction is ignored and will not have any effects on the current cycle. The Read Data instruction allows clock rates from D.C. to a maximum of fR (see *AC Electrical Characteristics*).

The Read Data (03h) instruction is only supported in Standard SPI mode.

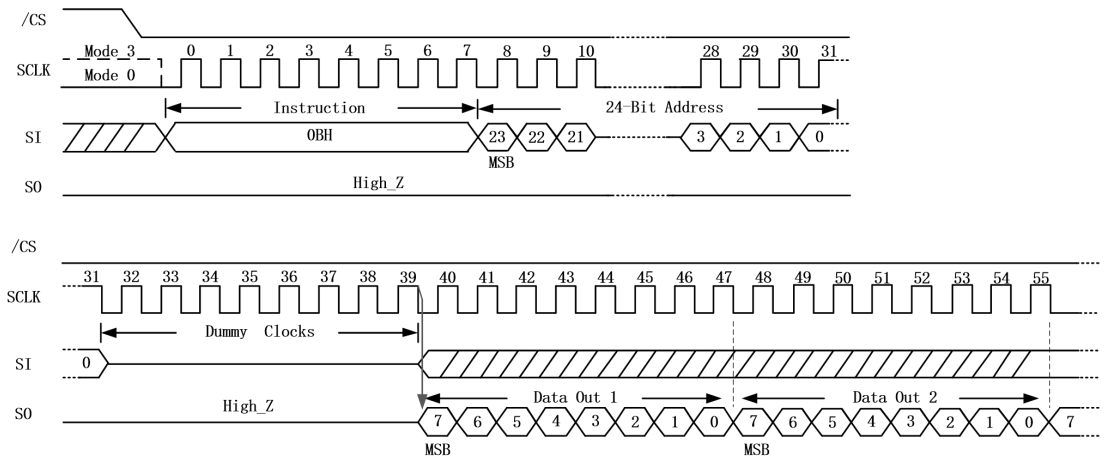
Figure 7.2.1**.** Read Data Instruction (SPI Mode only)



7.2.2 Fast Read (0BH)

The Fast Read instruction is similar to the *Read Data* instruction except that it can operate at the highest possible frequency of FR (see *AC Electrical Characteristics*). In standard SPI mode, this is accomplished by adding eight “dummy” clocks after the 24-bit address as shown in *Figure 7.2.2a*. The dummy clocks allow the devices internal circuits additional time for setting up the initial address. During the dummy clocks the data value on the SO pin is a “don’t care”.

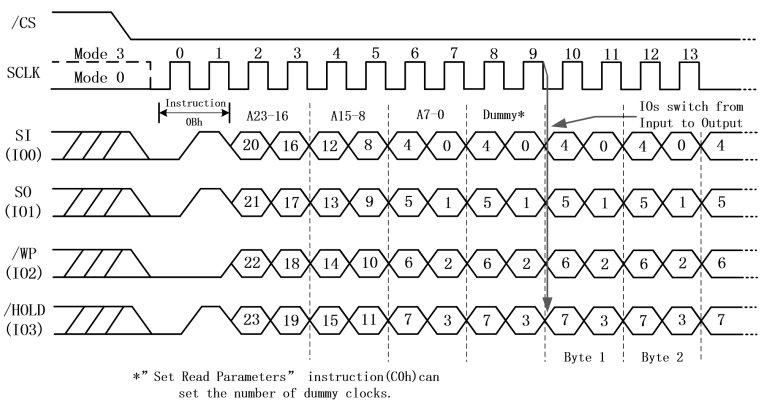
Figure 7.2.2a. Fast Read Instruction (SPI Mode)



Fast Read (0Bh) in QPI Mode

The Fast Read instruction is also supported in QPI mode. When QPI mode is enabled, the number of dummy clocks is configured by the “*Set Read Parameters (C0h)*” instruction to accommodate a wide range of applications with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P[5:4] setting, the number of dummy clocks can be configured as either 2, 4, 6 or 8. The default number of dummy clocks upon power up or after a Reset instruction is 2.

Figure 7.2.2b. Fast Read Instruction (QPI Mode)

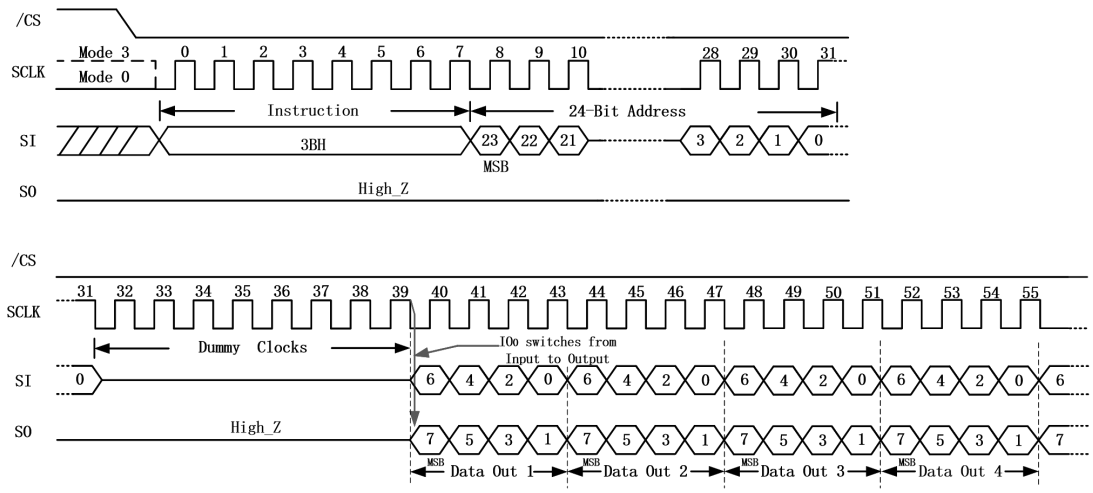


7.2.3 Fast Read Dual Output (3Bh)

The Fast Read Dual Output (3Bh) instruction is similar to the standard *Fast Read (0Bh)* instruction except that data is output on two pins; SI and SO. This allows data to be transferred at twice the rate of standard SPI devices. The Fast Read Dual Output instruction is ideal for quickly downloading code from Flash to RAM upon power-up or for applications that cache code-segments to RAM for execution.

Similar to the Fast Read instruction, the Fast Read Dual Output instruction can operate at the highest possible frequency of FR (see *AC Electrical Characteristics*). This is accomplished by adding eight “dummy” clocks after the 24-bit address as shown in *Figure 7.2.3*. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is “don’t care”. However, the SI pin should be high-impedance prior to the falling edge of the first data out clock.

Figure 7.2.3. Fast Read Dual Output Instruction (SPI Mode only)

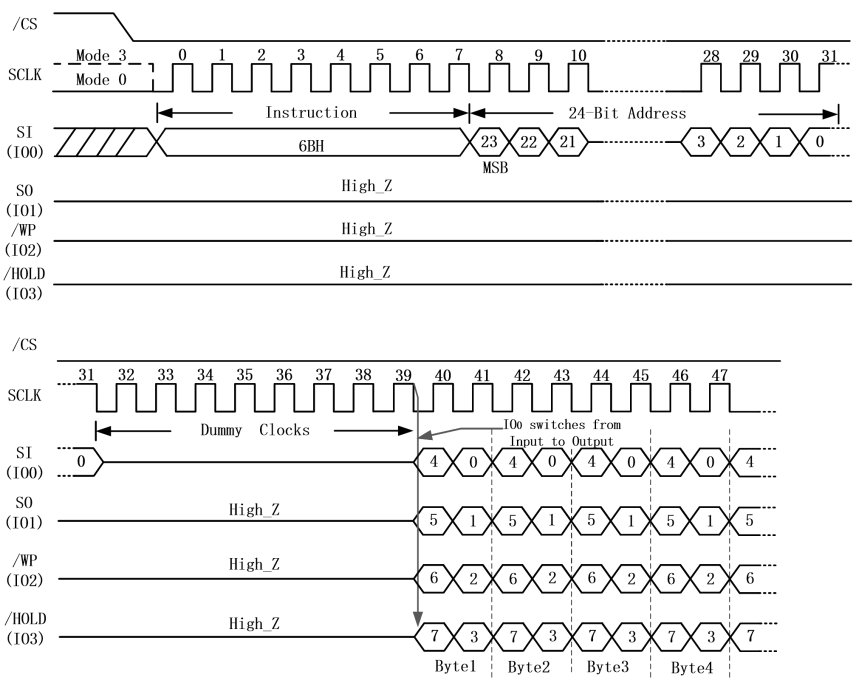


7.2.4 Fast Read Quad Output (6Bh)

The Fast Read Quad Output (6Bh) instruction is similar to the *Fast Read Dual Output (3Bh)* instruction except that data is output on four pins, SI, SO, /WP, and /HOLD. The Quad Enable (QE) bit in Status Register-2 must be set to 1 before the device will accept the Fast Read Quad Output Instruction. The Fast Read Quad Output Instruction allows data to be transferred at four times the rate of standard SPI devices.

The Fast Read Quad Output instruction can operate at the highest possible frequency of FR (see *AC Electrical Characteristics*). This is accomplished by adding eight “dummy” clocks after the 24-bit address as shown in *Figure 7.2.4*. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is “don’t care”. However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

Figure 7.2.4. Fast Read Quad Output Instruction (SPI Mode only)



7.2.5 Fast Read Dual I/O (BBh)

The Fast Read Dual I/O (BBh) instruction allows for improved random access while maintaining two IO pins, SI and SO. It is similar to the *Fast Read Dual Output (3Bh)* instruction but with the capability to input the Address bits (A23-0) two bits per clock. This reduced instruction overhead may allow for code execution (XIP) directly from the Dual SPI in some applications.

Fast Read Dual I/O with "Continuous Read Mode"

The Fast Read Dual I/O instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input Address bits (A23- 0), as shown in *Figure 7.2.5a*. The upper nibble of the (M7-4) controls the length of the next Fast Read Dual I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M5-4 = (1,0), then the next Fast Read Dual I/O instruction (after /CS is raised and then lowered) does not require the BBh instruction code, as shown in *Figure 7.2.5b*. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If the "Continuous Read Mode" bits M5-4 do not equal to (1,0), the next instruction (after /CS is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFFFh on SI for the next instruction (16 clocks), to ensure M4 = 1 and return the device to normal operation.

Figure 7.2.5a. Fast Read Dual I/O Instruction (Initial instruction or previous M5-4≠10, SPI Mode only)

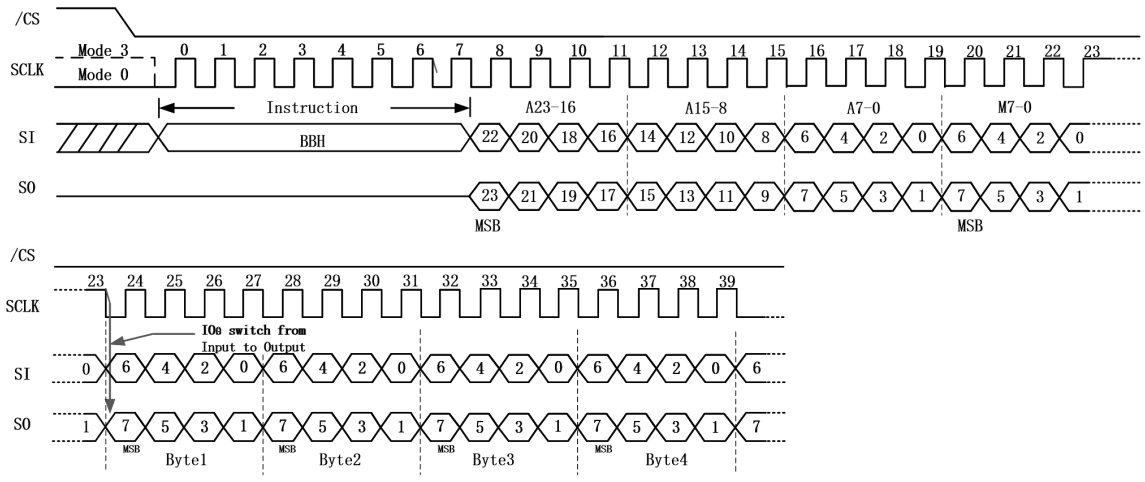
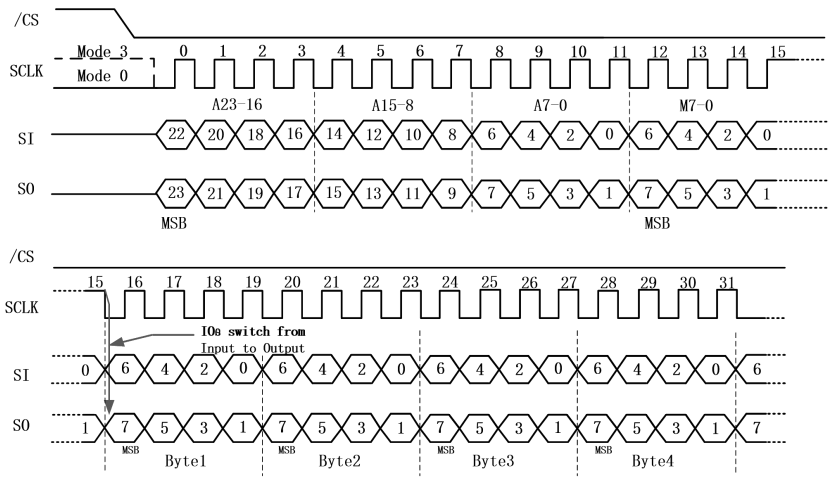


Figure 7.2.5b. Fast Read Dual I/O Instruction (Previous instruction set M5-4 = 10, SPI Mode only)



7.2.6 Fast Read Quad I/O (EBh)

The Fast Read Quad I/O (EBh) instruction is similar to the *Fast Read Dual I/O (BBh)* instruction except that address and data bits are input and output through four pins SI, SO, /WP and /HOLD and four Dummy clocks are required in SPI mode prior to the data output. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI. The Quad Enable bit (QE) of Status Register-2 must be set to enable the Fast Read Quad I/O Instruction.

Fast Read Quad I/O with "Continuous Read Mode"

The Fast Read Quad I/O instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input Address bits (A23-0), as shown in *Figure 7.2.6a*. The upper nibble of the (M7-4) controls the length of the next Fast Read Quad I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M5-4 = (1,0), then the next Fast Read Quad I/O instruction (after /CS is raised and then lowered) does not require the EBh instruction code, as shown in *Figure 7.2.6b*. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If the "Continuous Read Mode" bits M5-4 do not equal to (1,0), the next instruction (after /CS is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFh on SI for the next instruction (8 clocks), to ensure M4 = 1 and return the device to normal operation.

Figure 7.2.6a. Fast Read Quad I/O Instruction (Initial instruction or previous M5-4≠10, SPI Mode)

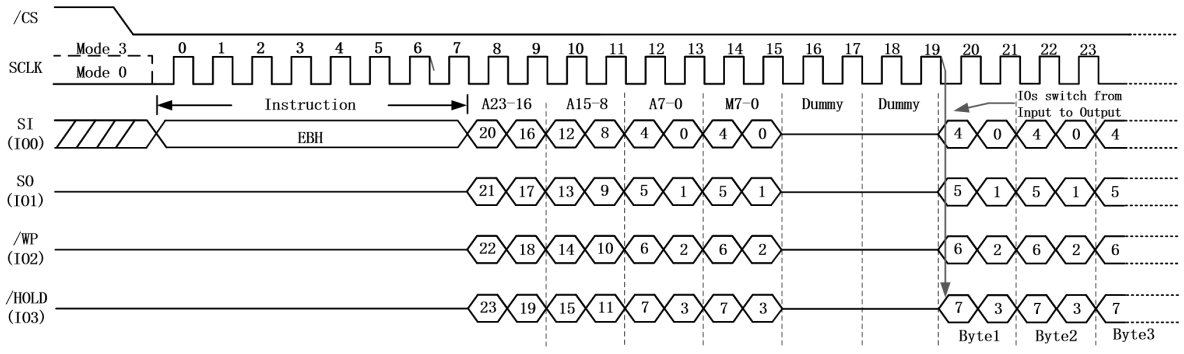
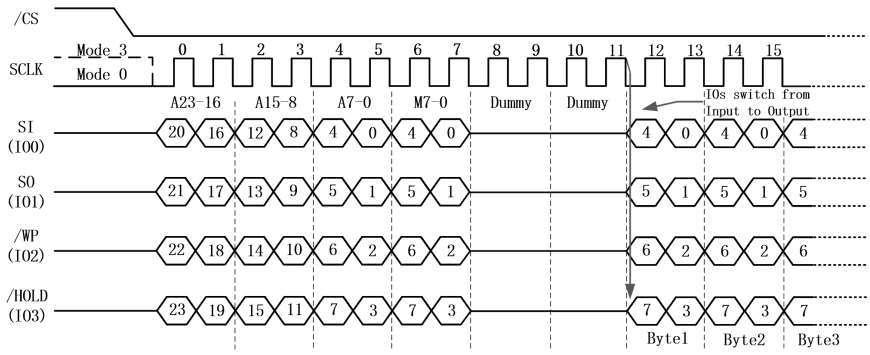


Figure 7.2.6b. Fast Read Quad I/O Instruction (Previous instruction set M5-4 = 10, SPI Mode)



Fast Read Quad I/O with "8/16/32/64-Byte Wrap Around" in Standard SPI mode

The Fast Read Quad I/O instruction can also be used to access a specific portion within a page by issuing a "*Set Burst with Wrap*" (77h) command prior to EBh. The "Set Burst with Wrap" (77h) command can either enable or disable the "Wrap Around" feature for the following EBh commands. When "Wrap Around" is enabled, the data being accessed can be limited to an 8, 16, 32 or 64-byte section of a 256-byte page. The output data starts at the initial address specified in the instruction, once it reaches the ending boundary of the 8/16/32/64- byte section, the output will wrap around to the beginning boundary automatically until /CS is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands.

The "Set Burst with Wrap" instruction allows three "Wrap Bits", W6-4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-5 are used to specify the length of the wrap around section within a page. Refer to *section 7.2.9* for detail descriptions.

Fast Read Quad I/O (EBh) in QPI Mode

The Fast Read Quad I/O instruction is also supported in QPI mode, as shown in *Figure 7.2.6c*. When QPI mode is enabled, the number of dummy clocks is configured by the "*Set Read Parameters (C0h)*" instruction to accommodate a wide range of applications with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P[5:4] setting, the number of dummy clocks can be configured as either 2, 4, 6 or 8. The default number of dummy clocks upon power up or after a Reset instruction is 2. In QPI mode, the "Continuous Read Mode" bits M7-0 are also considered as dummy clocks. In the default setting, the data output will follow the Continuous Read Mode bits immediately.

" Continuous Read Mode" feature is also available in QPI mode for Fast Read Quad I/O instruction. Please refer to the description on previous pages.

" Wrap Around" feature is not available in QPI mode for Fast Read Quad I/O instruction. To perform a read operation with fixed data length wrap around in QPI mode, a dedicated "*Burst Read with Wrap*" (0Ch) instruction must be used. Please refer to *section 7.2.10* for details.

Figure 7.2.6c. Fast Read Quad I/O Instruction (Initial instruction or previous M5-4 ≠ 10, QPI Mode)

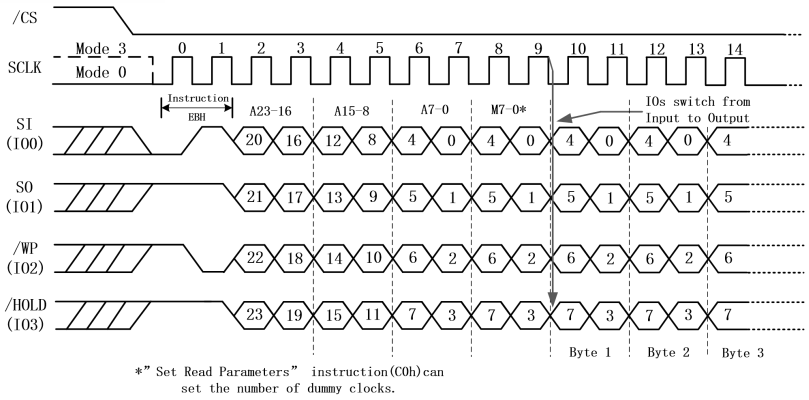
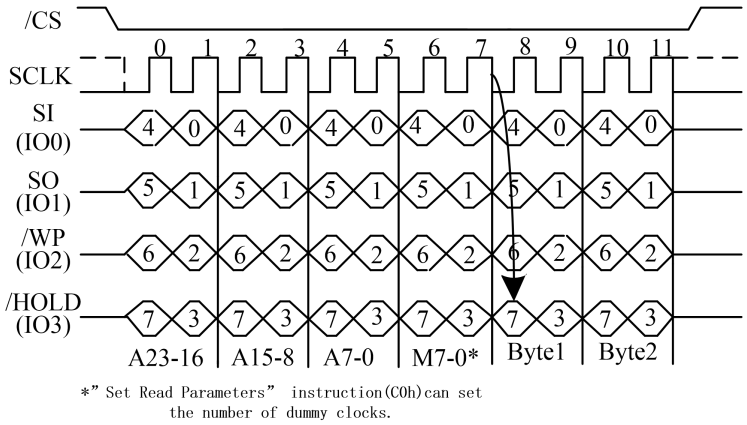


Figure 7.2.6d. Fast Read Quad I/O Instruction (Initial instruction or previous M5-4 = 10, QPI Mode)



7.2.7 Word Read Quad I/O (E7h)

The Word Read Quad I/O (E7h) instruction is similar to the *Fast Read Quad I/O (EBh)* instruction except that the lowest Address bit (A0) must equal 0 and only two Dummy clocks are required prior to the data output. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI. The Quad Enable bit (QE) of Status Register-2 must be set to enable the Word Read Quad I/O Instruction.

Word Read Quad I/O with "Continuous Read Mode"

The Word Read Quad I/O instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input Address bits (A23-0), as shown in *Figure 7.2.7a*. The upper nibble of the (M7-4) controls the length of the next Word Read Quad I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M5-4 = (1,0), then the next Word Read Quad I/O instruction (after /CS is raised and then lowered) does not require the E7h instruction code, as shown in *Figure 7.2.7b*. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If the "Continuous Read Mode" bits M5-4 do not equal to (1,0), the next instruction (after /CS is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFh on SI for the next instruction (8 clocks), to ensure M4 = 1 and return the device to normal operation.

Figure 7.2.7a. Word Read Quad I/O Instruction (Initial instruction or previous M5-4 ≠ 10, SPI Mode only)

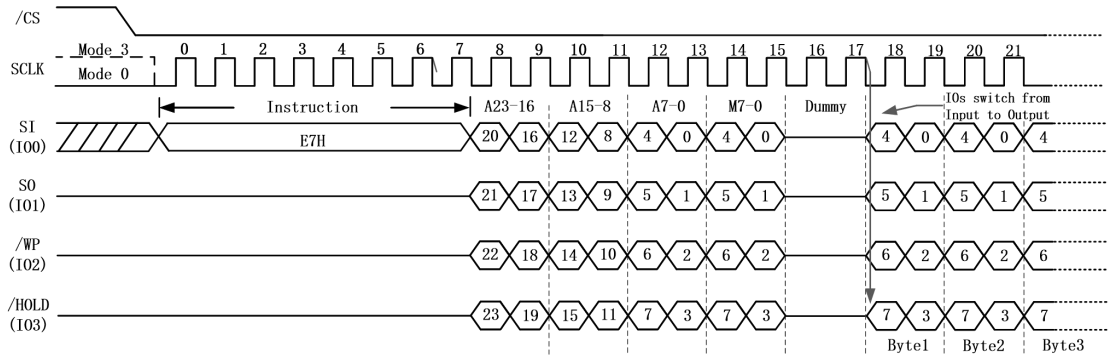
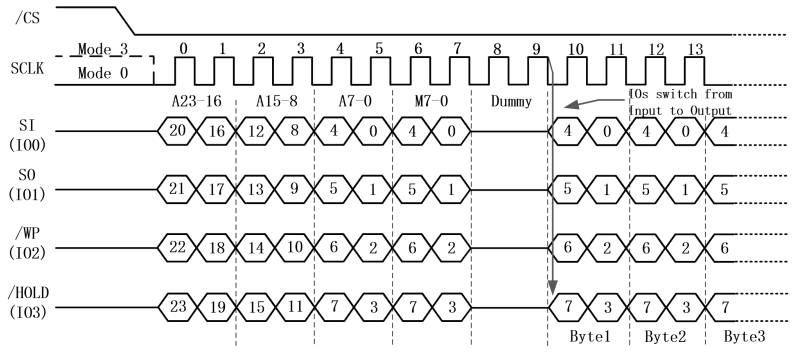


Figure 7.2.7b. Word Read Quad I/O Instruction (Previous instruction set M5-4 = 10, SPI Mode only)



Word Read Quad I/O with "8/16/32/64-Byte Wrap Around" in Standard SPI mode

The Word Read Quad I/O instruction can also be used to access a specific portion within a page by issuing a "*Set Burst with Wrap*" (77h) command prior to E7h. The "Set Burst with Wrap" (77h) command can either enable or disable the "Wrap Around" feature for the following E7h commands. When "Wrap Around" is enabled, the data being accessed can be limited to either an 8, 16, 32 or 64-byte section of a 256-byte page. The output data starts at the initial address specified in the instruction, once it reaches the ending boundary of the 8/16/32/64- byte section, the output will wrap around to the beginning boundary automatically until /CS is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands.

The "Set Burst with Wrap" instruction allows three "Wrap Bits", W6-4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-5 are used to specify the length of the wrap around section within a page. See *section 7.2.9* for detail descriptions.

7.2.8 Octal Word Read Quad I/O (E3h)

The Octal Word Read Quad I/O (E3h) instruction is similar to the *Fast Read Quad I/O (EBh)* instruction except that the lower four Address bits (A0, A1, A2, A3) must equal 0. As a result, the dummy clocks are not required, which further reduces the instruction overhead allowing even faster random access for code execution (XIP). The Quad Enable bit (QE) of Status Register-2 must be set to enable the Octal Word Read Quad I/O Instruction.

Octal Word Read Quad I/O with "Continuous Read Mode"

The Octal Word Read Quad I/O instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7- 0) after the input Address bits (A23-0), as shown in *Figure 7.2.8a*. The upper nibble of the (M7-4) controls the length of the next Octal Word Read Quad I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M5-4 = (1,0), then the next Octal Word Read Quad I/O instruction (after /CS is raised and then lowered) does not require the E3h instruction code, as shown in *Figure 7.2.8b*. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If the "Continuous Read Mode" bits M5-4 do not equal to (1,0), the next instruction (after /CS is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFh on SI for the next instruction (8 clocks), to ensure M4 = 1 and return the device to normal operation.

Figure 7.2.8a. Octal Word Read Quad I/O Instruction (Initial instruction or previous M5-4 ≠ 10, SPI Mode only)

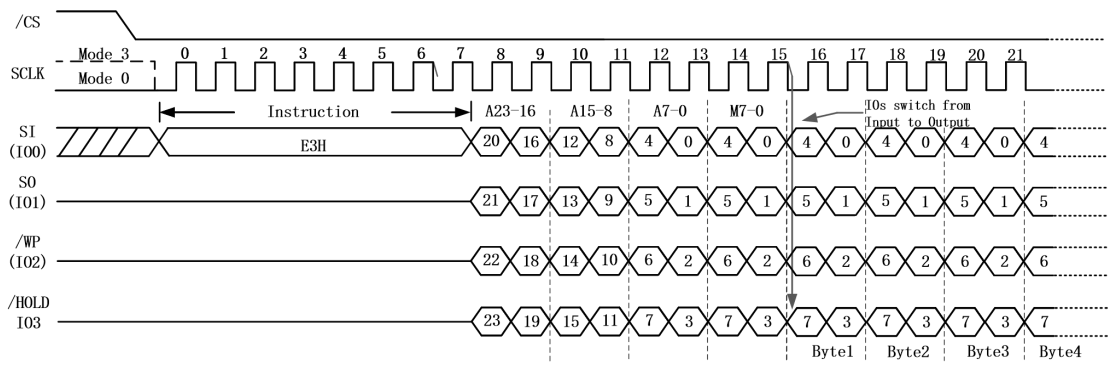
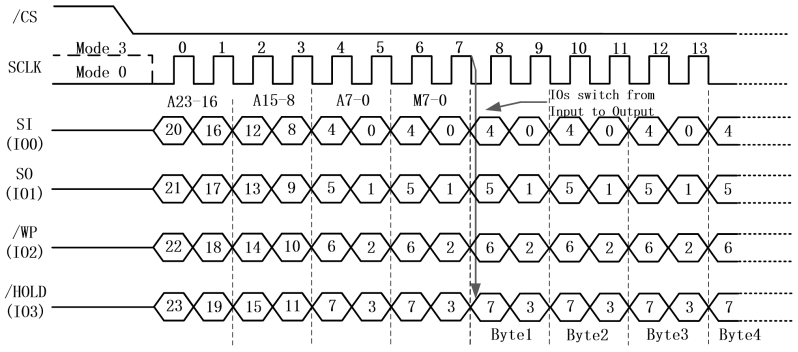


Figure 7.2.8b. Octal Word Read Quad I/O Instruction (Previous instruction set M5-4 = 10, SPI Mode only)



7.2.9 Set Burst with Wrap (77h)

In Standard SPI mode, the Set Burst with Wrap (77h) instruction is used in conjunction with "*Fast Read Quad I/O (EBh)*", "*Word Read Quad I/O (E7h)*" and "*Octal Word Read Quad I/O (E3h)*" instructions to access a fixed length of 8/16/32/64-byte section within a 256-byte page. Certain applications can benefit from this feature and improve the overall system code execution performance.

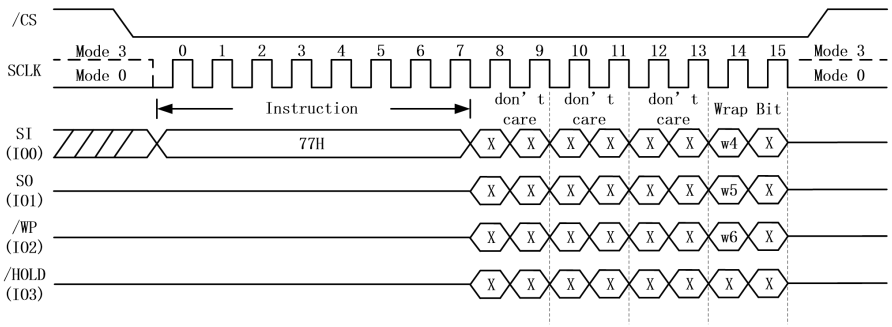
Similar to a Quad I/O instruction, the Set Burst with Wrap instruction is initiated by driving the /CS pin low and then shifting the instruction code "77h" followed by 24 dummy bits and 8 "Wrap Bits", W7-0. The instruction sequence is shown in *Figure 7.2.9*. Wrap bit W7 and the lower nibble W3-0 are not used.

W6, W5	W4 = 0		W4 =1 (DEFAULT)	
	Wrap Around	Wrap Length	Wrap Around	Wrap Length
0 0	Yes	8-byte	No	N/A
0 1	Yes	16-byte	No	N/A
1 0	Yes	32-byte	No	N/A
1 1	Yes	64-byte	No	N/A

Once W6-4 is set by a Set Burst with Wrap instruction, all the following "*Fast Read Quad I/O (EBh)*", "*Word Read Quad I/O (E7h)*" and "*Octal Word Read Quad I/O (E3h)*" instructions will use the W6-4 setting to access the 8/16/32/64-byte section within any page. To exit the "Wrap Around" function and return to normal read operation, another Set Burst with Wrap instruction should be issued to set W4 = 1. The default value of W4 upon power on or after a software/hardware reset is 1.

In QPI mode, the "Burst Read with Wrap (0CH)" command should be used to perform the Read Operation with "Wrap Around" feature. The Wrap Length must be re-configured by "Set Read Parameters (C0H) command.

Figure 7.2.9. Set Burst with Wrap Instruction (SPI Mode only)

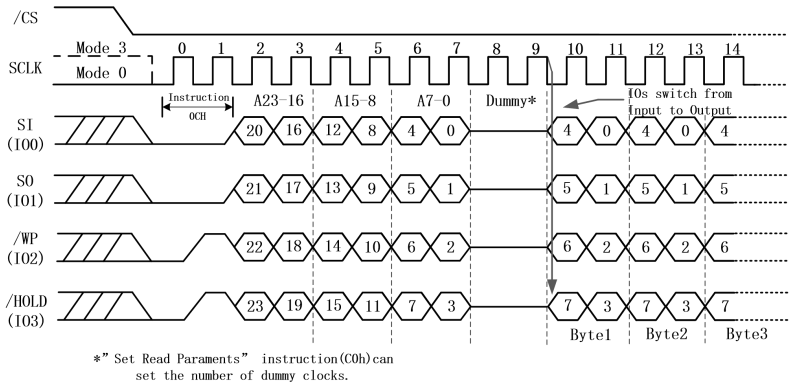


7.2.10 Burst Read with Wrap (0Ch)

The “Burst Read with Wrap (0Ch)” instruction provides an alternative way to perform the read operation with “Wrap Around” in QPI mode. The instruction is similar to the “*Fast Read (0Bh)*” instruction in QPI mode, except the addressing of the read operation will “Wrap Around” to the beginning boundary of the “Wrap Length” once the ending boundary is reached.

The “Wrap Length” and the number of dummy clocks can be configured by the “*Set Read Parameters (C0h)*” instruction.

Figure 7.2.10. Burst Read with Wrap Instruction (QPI Mode only)



7.3 ID and Power Instructions

7.3.1 Power-down (B9h)

Although the standby current during normal operation is relatively low, standby current can be further reduced with the Power-down instruction. The lower power consumption makes the Power-down instruction especially useful for battery powered applications (See ICC1 and ICC2 in *AC Characteristics*). The instruction is initiated by driving the /CS pin low and shifting the instruction code “B9h” as shown in *Figure 7.3.1a* (SPI mode) & *Figure 7.3.1b* (QPI mode).

The /CS pin must be driven high after the eighth bit has been latched. If this is not done the Power-down instruction will not be executed. After /CS is driven high, the power- down state will entered within the time duration of tDP (See *AC Characteristics*). While in the power-down state only the *Release Power-down / Device ID (ABh)* instruction, software reset sequence or hardware reset sequence, which restores the device to normal operation, will be recognized. All other instructions are ignored. This includes the Read Status Register instruction, which is always available during normal operation. Ignoring all but one instruction makes the Power Down state a useful condition for securing maximum write protection. The device always powers-up in the normal operation with the standby current of ICC1

Figure 7.3.1a. Deep Power-down Instruction (SPI Mode)

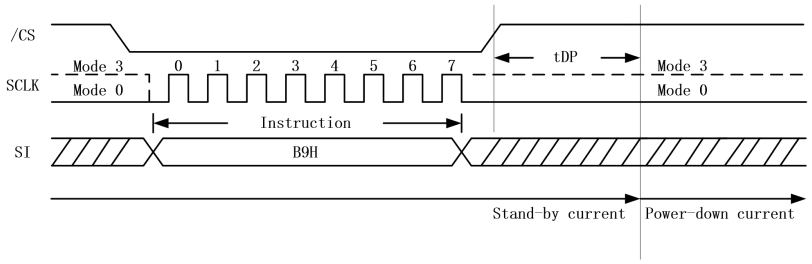
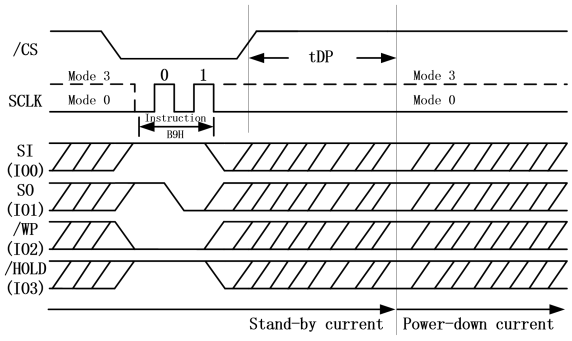


Figure 7.3.1b. Deep Power-down Instruction (QPI Mode)



7.3.2 Release Power-down / Device ID (ABh)

The Release from Power-down / Device ID instruction is a multi-purpose instruction. It can be used to release the device from the power-down state, or obtain the devices electronic identification (ID) number.

To release the device from the power- down state, the instruction is issued by driving the /CS pin low, shifting the instruction code “ABh” and driving /CS high as shown in *Figure 7.3.2a* (SPI mode) & *Figure 7.3.2b* (QPI mode). Release from power-down will take the time duration of tRES1 (See *AC Characteristics*) before the device will resume normal operation and other instructions are accepted. The /CS pin must remain high during the tRES1 time duration.

When used only to obtain the Device ID while not in the power-down state, the instruction is initiated by driving the /CS pin low and shifting the instruction code “ABh” followed by 3-dummy bytes. The Device ID bits are then shifted out on the falling edge of SCLK with most significant bit (MSB) first. The Device ID value for the BY25Q64AL is listed in *Manufacturer and Device Identification table*. The Device ID can be read continuously. The instruction is completed by driving /CS high.

When used to release the device from the power-down state and obtain the Device ID, the instruction is the same as previously described, and shown in *Figure 7.3.2c* (SPI mode) & *Figure 7.3.2d* (QPI mode), except that after /CS is driven high it must remain high for a time duration of tRES2 (See *AC Characteristics*) . After this time duration the device will resume normal operation and other instructions will be accepted. If the Release from Power- down / Device ID instruction is issued while an Erase, Program or Write cycle is in process (when BUSY equals 1) the instruction is ignored and will not have any effects on the current cycle.

Figure 7.3.2a. Release Power-down Instruction (SPI Mode)

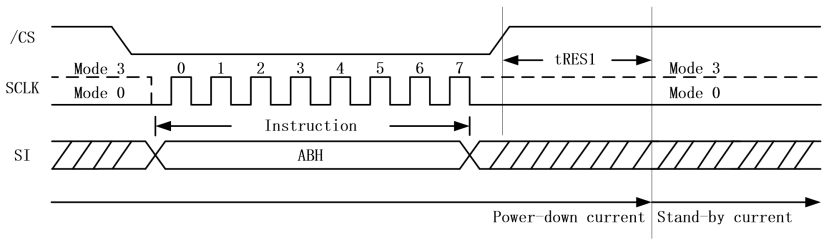


Figure 7.3.2b. Release Power-down Instruction (QPI Mode)

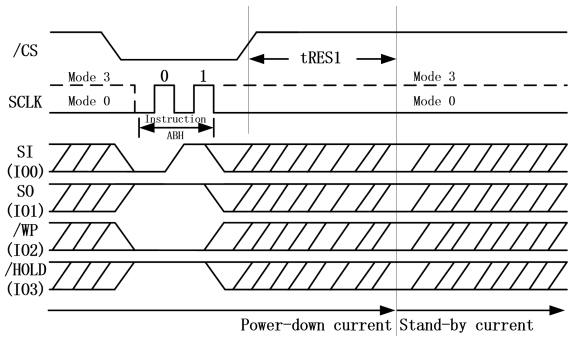


Figure 7.3.2c. Release Power-down / Device ID Instruction (SPI Mode)

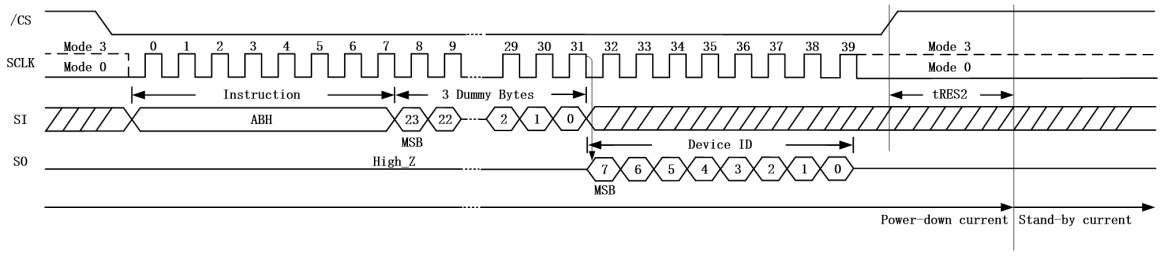
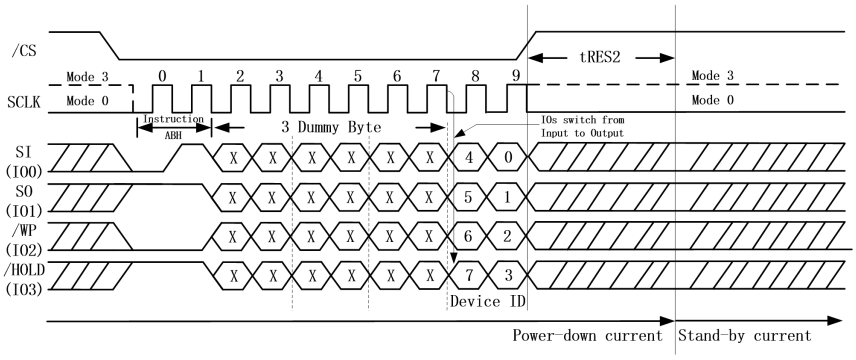


Figure 7.3.2d. Release Power-down / Device ID Instruction (QPI Mode)



7.3.3 Read Manufacturer / Device ID (90h)

The Read Manufacturer/Device ID instruction is an alternative to the *Release from Power-down / Device ID* instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID.

The Read Manufacturer/Device ID instruction is very similar to the *Release from Power-down / Device ID* instruction. The instruction is initiated by driving the /CS pin low and shifting the instruction code “90h” followed by a 24-bit address (A23-A0) of 000000h. After which, the Manufacturer ID for BY Technology (68h) and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in *Figure 7.3.3*. The Device ID values for the BY25Q64AL are listed in *Manufacturer and Device Identification table*. If the 24-bit address is initially set to 000001h the Device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving /CS high.

Figure 7.3.3a. Read Manufacturer / Device ID Instruction (SPI Mode)

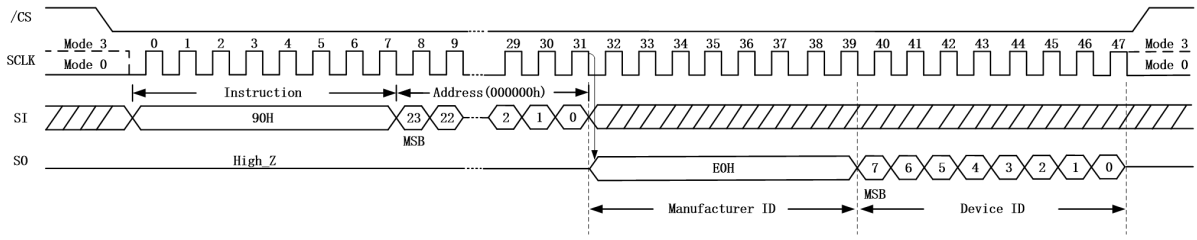
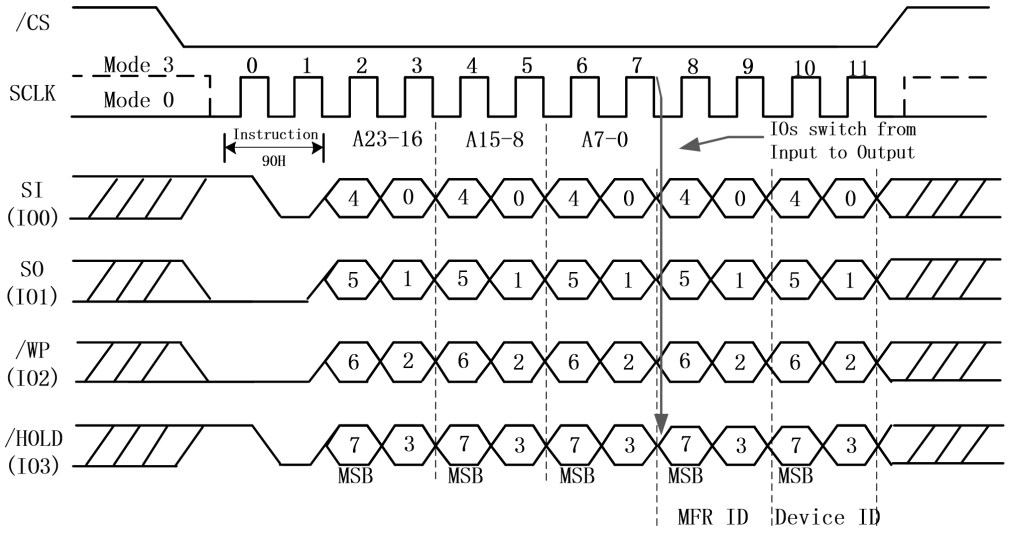


Figure 7.3.3b. Read Manufacturer / Device ID Instruction (QPI Mode)

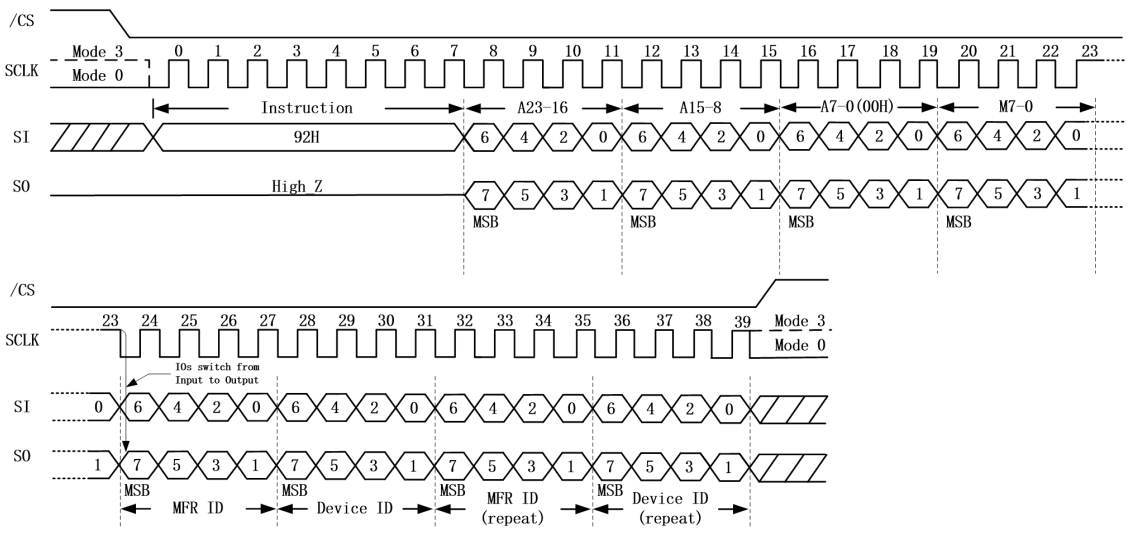


7.3.4 Read Manufacturer / Device ID Dual I/O (92h)

The Read Manufacturer / Device ID Dual I/O instruction is an alternative to the *Read Manufacturer / Device ID* instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID at 2x speed.

The Read Manufacturer / Device ID Dual I/O instruction is similar to the *Fast Read Dual I/O* instruction. The instruction is initiated by driving the /CS pin low and shifting the instruction code "92h" followed by a 24-bit address (A23-A0) of 000000h and "Continuous Read Mode" bits (M7-M0), but with the capability to input the Address bits two bits per clock. After which, the Manufacturer ID for BY Technology (68h) and the Device ID are shifted out 2 bits per clock on the falling edge of SCLK with most significant bits (MSB) first as shown in *Figure 7.3.4*. The Device ID values for the BY25Q64AL are listed in *Manufacturer and Device Identification table*. If the 24-bit address is initially set to 000001h the Device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving /CS high.

Figure 7.3.4. Read Manufacturer / Device ID Dual I/O Instruction (SPI Mode only)

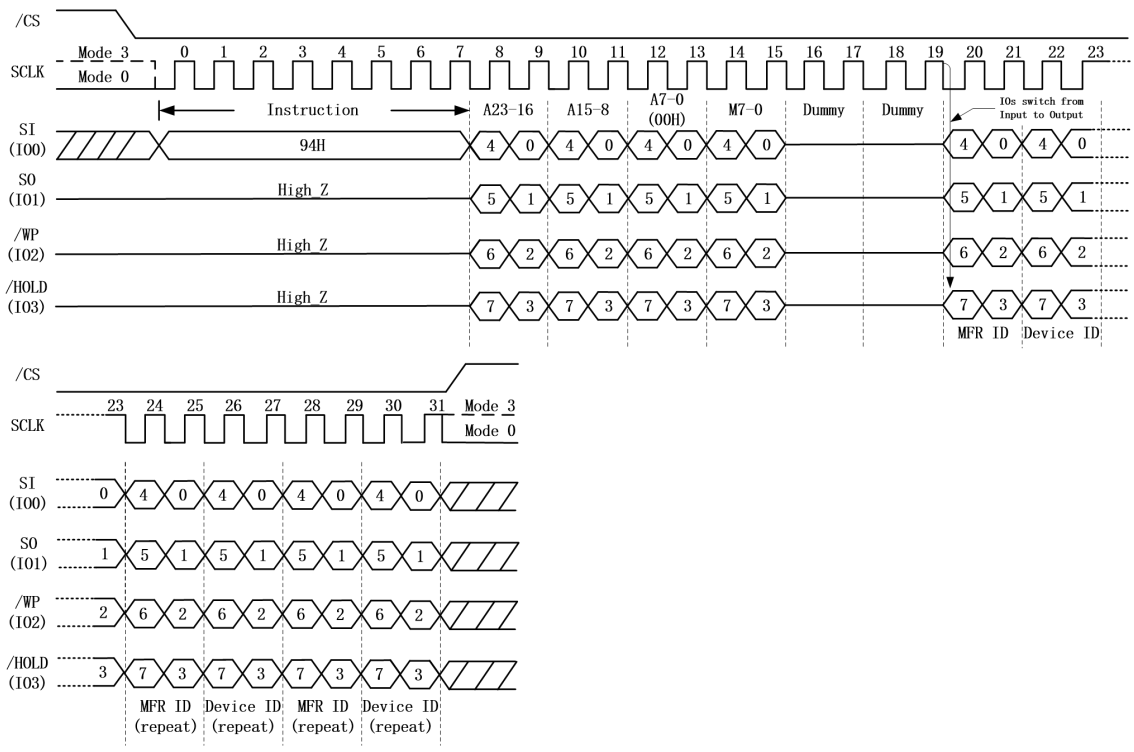


7.3.5 Read Manufacturer / Device ID Quad I/O (94h)

The Read Manufacturer / Device ID Quad I/O instruction is an alternative to the *Read Manufacturer / Device ID* instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID at 4x speed.

The Read Manufacturer / Device ID Quad I/O instruction is similar to the *Fast Read Quad I/O* instruction. The instruction is initiated by driving the /CS pin low and shifting the instruction code "94h" followed by a 24-bit address (A23-A0) of 000000h and "Continuous Read Mode" bits (M7-M0) and a four clock dummy cycles, but with the capability to input the Address bits four bits per clock. After which, the Manufacturer ID for BY Technology (68h) and the Device ID are shifted out four bits per clock on the falling edge of SCLK with most significant bit (MSB) first as shown in *Figure 7.3.5*. The Device ID values for the BY25Q64AL are listed in *Manufacturer and Device Identification table*. If the 24-bit address is initially set to 000001h the Device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving /CS high.

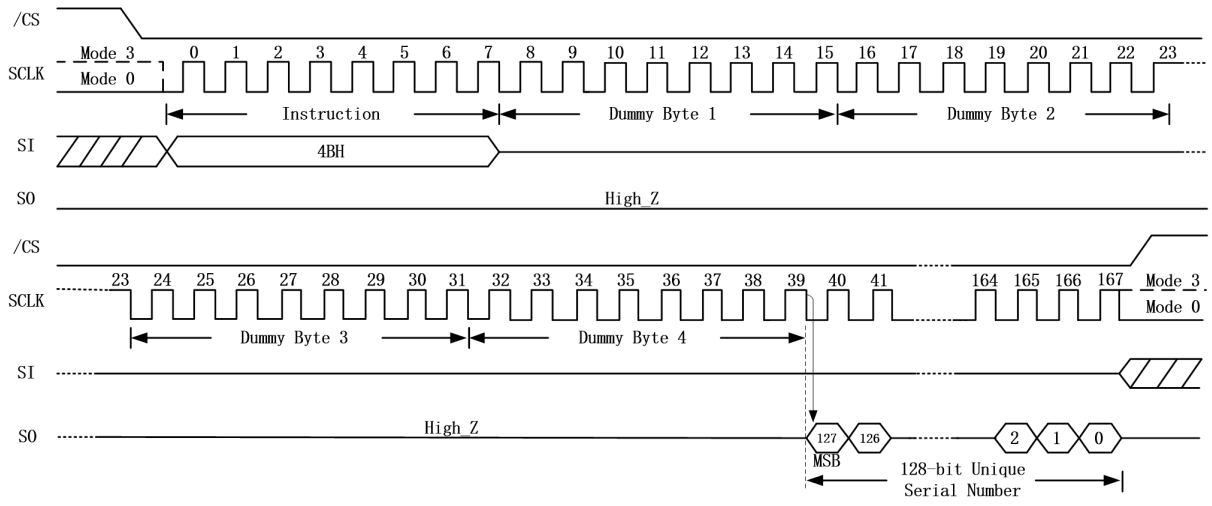
Figure 7.3.5. Read Manufacturer / Device ID Quad I/O Instruction (SPI Mode only)



7.3.6 Read Unique ID Number (4Bh)

The Read Unique ID Number instruction accesses a factory-set read-only 128-bit number that is unique to each BY25Q64AL device. The ID number can be used in conjunction with user software methods to help prevent copying or cloning of a system. The Read Unique ID instruction is initiated by driving the /CS pin low and shifting the instruction code “4Bh” followed by a four bytes of dummy clocks. After which, the 128-bit ID is shifted out on the falling edge of SCLK as shown in *Figure 7.3.6*.

Figure 7.3.6. Read Unique ID Number Instruction (SPI Mode only)



7.3.7 Read JEDEC ID (9Fh)

For compatibility reasons, the BY25Q64AL provides several instructions to electronically determine the identity of the device. The Read JEDEC ID instruction is compatible with the JEDEC standard for SPI compatible serial memories that was adopted in 2003. The instruction is initiated by driving the /CS pin low and shifting the instruction code “9Fh”. The JEDEC assigned Manufacturer ID byte for BY Technology (68h) and two Device ID bytes, Memory Type (ID15-ID8) and Capacity (ID7-ID0) are then shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in *Figure 7.3.7a* (SPI mode) & *Figure 7.3.7b* (QPI mode). For memory type and capacity values refer to *Manufacturer and Device Identification table*.

Figure 7.3.7a. Read JEDEC ID Instruction (SPI Mode)

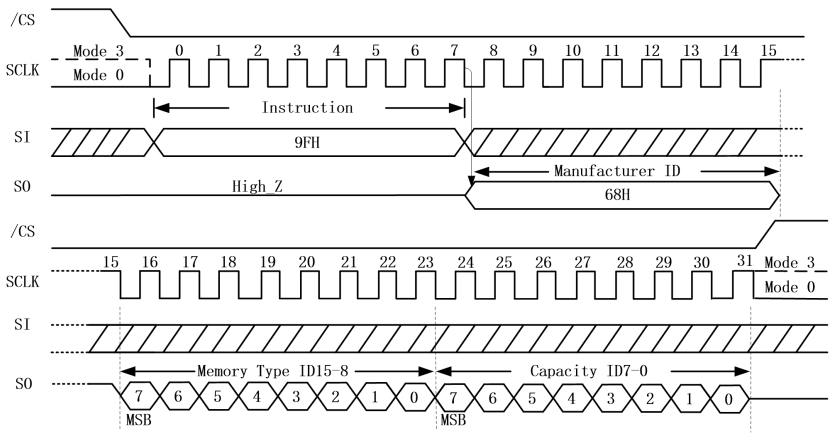
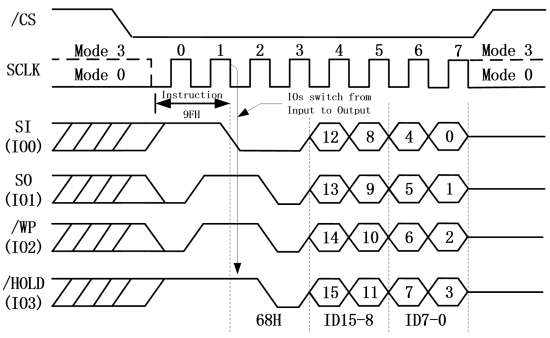


Figure 7.3.7b. Read JEDEC ID Instruction (QPI Mode)



7.4 Program / Erase and Security Instructions

7.4.1 Page Program (02h)

The Page Program instruction allows from one byte to 256 bytes (a page) of data to be programmed at previously erased (FFh) memory locations. A *Write Enable* instruction must be executed before the device will accept the Page Program Instruction (Status Register bit WEL= 1). The instruction is initiated by driving the /CS pin low then shifting the instruction code “02h” followed by a 24-bit address (A23-A0) and at least one data byte, into the SI pin. The /CS pin must be held low for the entire length of the instruction while data is being sent to the device. The Page Program instruction sequence is shown in *Figure 7.4.1a* (SPI mode) and *Figure 7.4.1b* (QPI mode).

If an entire 256 byte page is to be programmed, the last address byte (the 8 least significant address bits) should be set to 0. If the last address byte is not zero, and the number of clocks exceeds the remaining page length, the addressing will wrap to the beginning of the page. In some cases, less than 256 bytes (a partial page) can be programmed without having any effect on other bytes within the same page. One condition to perform a partial page program is that the number of clocks cannot exceed the remaining page length. If more than 256 bytes are sent to the device the addressing will wrap to the beginning of the page and overwrite previously sent data.

As with the write and erase instructions, the /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Page Program instruction will not be executed. After /CS is driven high, the self-timed Page Program instruction will commence for a time duration of tPP (See *AC Characteristics*). While the Page Program cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Page Program cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Page Program cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Page Program instruction will not be executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits or the Dynamic Protection Block/Sector Locks.

Figure 7.4.1a. Page Program Instruction (SPI Mode)

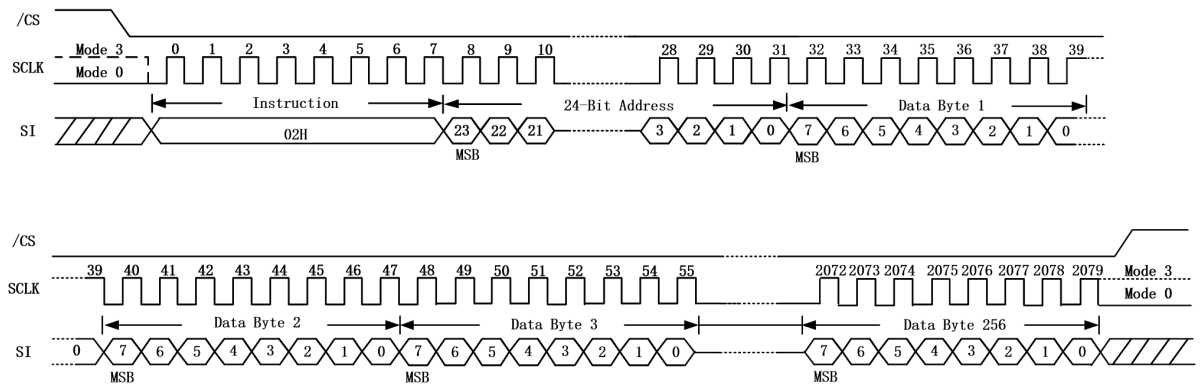
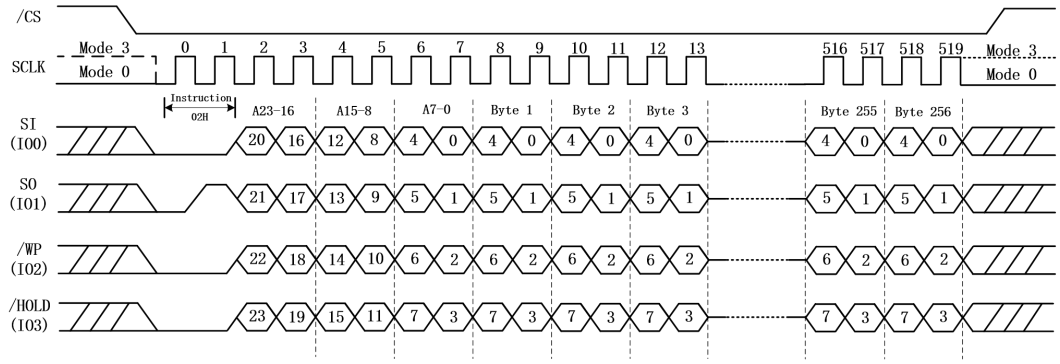


Figure 7.4.1b. Page Program Instruction (QPI Mode)

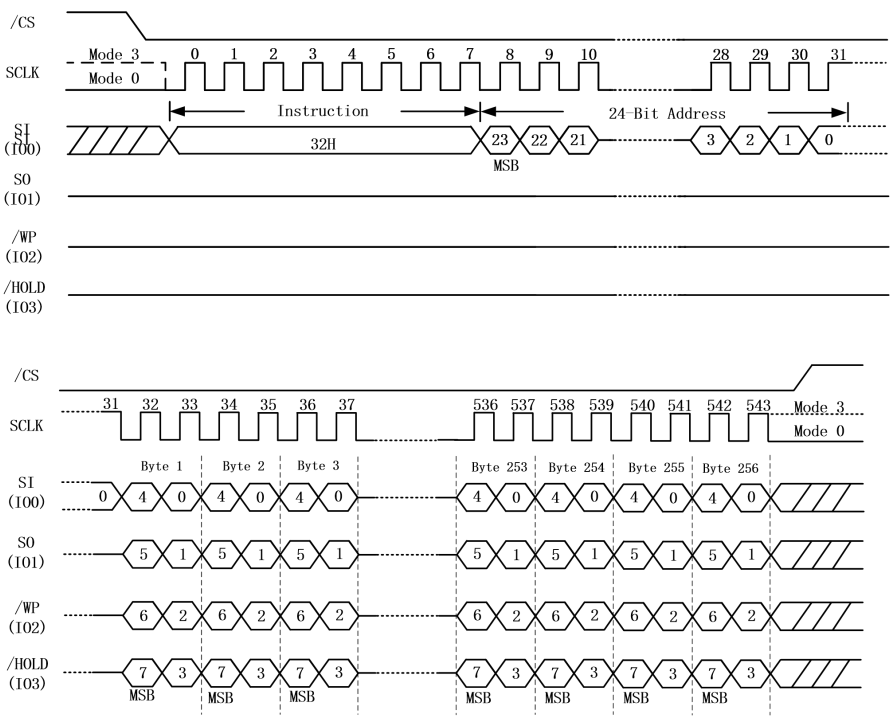


7.4.2 Quad Input Page Program (32h)

The Quad Page Program instruction allows up to 256 bytes of data to be programmed at previously erased (FFh) memory locations using four pins: SI, SO, /WP, and /HOLD. The Quad Page Program can improve performance for PROM Programmer and applications that have slow clock speeds <5MHz. Systems with faster clock speed will not realize much benefit for the Quad Page Program instruction since the inherent page program time is much greater than the time it take to clock-in the data.

To use Quad Page Program the Quad Enable (QE) bit in Status Register-2 must be set to 1. A *Write Enable* instruction must be executed before the device will accept the Quad Page Program instruction (Status Register-1, WEL=1). The instruction is initiated by driving the /CS pin low then shifting the instruction code “32h” followed by a 24-bit address (A23-A0) and at least one data byte, into the IO pins. The /CS pin must be held low for the entire length of the instruction while data is being sent to the device. All other functions of Quad Page Program are identical to standard Page Program. The Quad Page Program instruction sequence is shown in *Figure 7.4.2*.

Figure 7.4.2. Quad Input Page Program Instruction (SPI Mode only)



7.4.3 Sector Erase (20h)

The Sector Erase instruction sets all memory within a specified sector (4K-bytes) to the erased state of all 1s (FFh). A *Write Enable* instruction must be executed before the device will accept the Sector Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “20h” followed a 24-bit sector address (A23-A0). The Sector Erase instruction sequence is shown in *Figure 7.4.3a* (SPI mode) & *Figure 7.4.3b* (QPI mode).

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Sector Erase instruction will not be executed. After /CS is driven high, the self-timed Sector Erase instruction will commence for a time duration of tSE (See *AC Characteristics*). While the Sector Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Sector Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Sector Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Sector Erase instruction will not be executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits or the Dynamic Protection Block/Sector Locks.

Figure 7.4.3a. Sector Erase Instruction (SPI Mode)

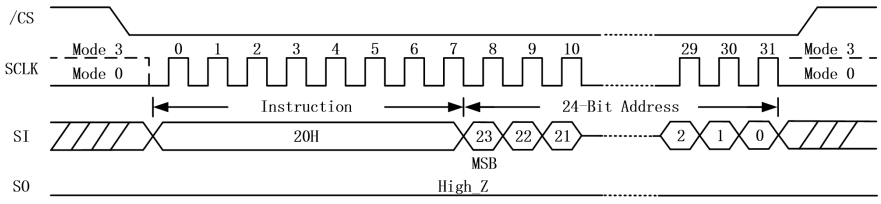
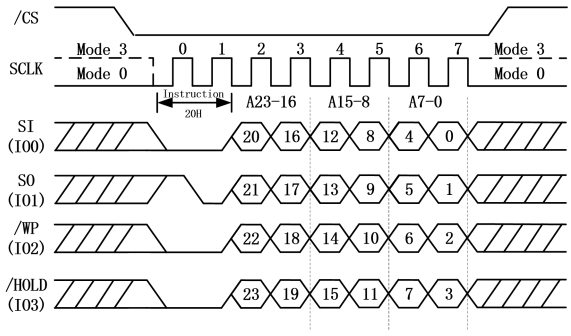


Figure 7.4.3b. Sector Erase Instruction (QPI Mode)



7.4.4 32KB Block Erase (52h)

The 32KB Block Erase instruction sets all memory within a specified block (32K-bytes) to the erased state of all 1s (FFh). A *Write Enable* instruction must be executed before the device will accept the 32KB Block Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “52h” followed a 24-bit block address (A23-A0). The Block Erase instruction sequence is shown in *Figure 7.4.4a* (SPI mode) & *Figure 7.4.4b* (QPI mode).

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the 32KB Block Erase instruction will not be executed. After /CS is driven high, the self-timed 32KB Block Erase instruction will commence for a time duration of tBE1 (See *AC Characteristics*). While the 32KB Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the 32KB Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the 32KB Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The 32KB Block Erase instruction will not be executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits or the Dynamic Protection Block/Sector Locks.

Figure 7.4.4a. 32KB Block Erase Instruction (SPI Mode)

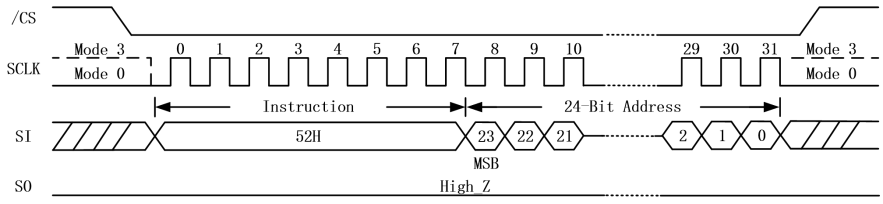
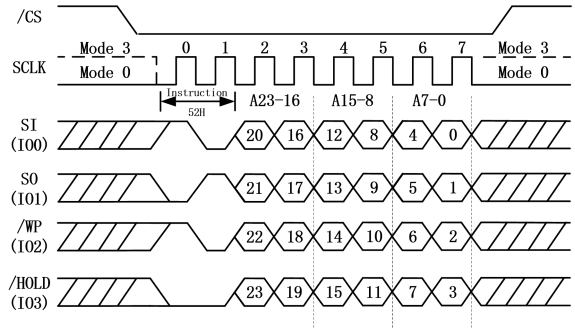


Figure 7.4.4b. 32KB Block Erase Instruction (QPI Mode)



7.4.5 64KB Block Erase (D8h)

The 64KB Block Erase instruction sets all memory within a specified block (64K-bytes) to the erased state of all 1s (FFh). A *Write Enable* instruction must be executed before the device will accept the 64KB Block Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “D8h” followed a 24-bit block address (A23-A0). The 64KB Block Erase instruction sequence is shown in *Figure 7.4.5a* (SPI mode) & *Figure 7.4.5b* (QPI mode).

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the 64KB Block Erase instruction will not be executed. After /CS is driven high, the self-timed 64KB Block Erase instruction will commence for a time duration of tBE (See *AC Characteristics*) . While the 64KB Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the 64KB Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the 64KB Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The 64KB Block Erase instruction will not be executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits or the Dynamic Protection Block/Sector Locks.

Figure 7.4.5a. 64KB Block Erase Instruction (SPI Mode)

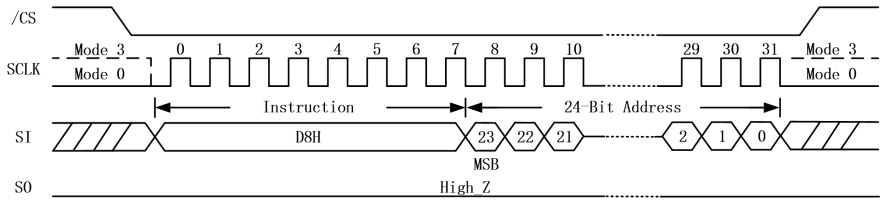
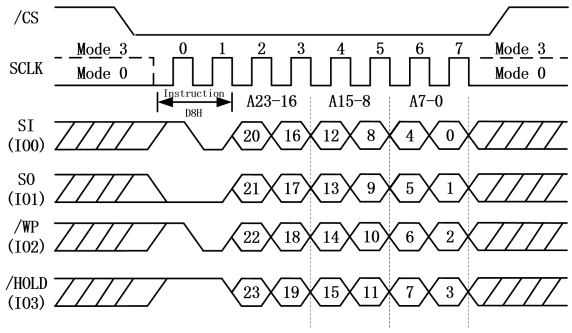


Figure 7.4.5b. 64KB Block Erase Instruction (QPI Mode)

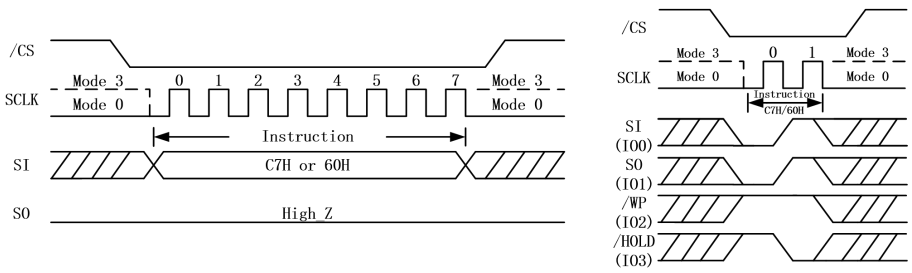


7.4.6 Chip Erase (C7h / 60h)

The Chip Erase instruction sets all memory within the device to the erased state of all 1s (FFh). A *Write Enable* instruction must be executed before the device will accept the Chip Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “C7h” or “60h”. The Chip Erase instruction sequence is shown in Figure 7.4.6.

The /CS pin must be driven high after the eighth bit has been latched. If this is not done the Chip Erase instruction will not be executed. After /CS is driven high, the self-timed Chip Erase instruction will commence for a time duration of tCE (See *AC Characteristics*). While the Chip Erase cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Chip Erase cycle and becomes a 0 when finished and the device is ready to accept other instructions again. After the Chip Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Chip Erase instruction will not be executed if any memory region is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits or the Dynamic Protection Block/Sector Locks.

Figure 7.4.6. Chip Erase Instruction for SPI Mode (left) or QPI Mode (right)



7.4.7 Erase/Program Suspend (75h)

The Erase/Program Suspend instruction “75h”, allows the system to interrupt a program or Sector or Block Erase operation and then read from or program data to, any other sectors or blocks. The Erase/Program Suspend instruction sequence is shown in *Figure 7.4.7a* (SPI mode) & *Figure 7.4.7b* (QPI mode).

The Write Status Register instruction (01h, 31h, 11h) and Erase instructions (20h, 52h, D8h, C7h, 60h, 44h) and page program instruction are not allowed during Erase/Program Suspend. Erase/Program Suspend is valid only during the page program or Sector or 32KB/64KB Block erase operation. If written during the Chip Erase operation, the Erase/Program Suspend instruction is ignored.

The Erase/Program Suspend instruction “75h” will be accepted by the device only if the SUS1 bit or SUS2 bit in the Status Register equals to 0 and the BUSY bit equals to 1 while a page program or a Sector or 32KB/64KB Block Erase operation is on-going. If the SUS1 bit or SUS2 bit equals to 1 or the BUSY bit equals to 0, the Suspend instruction will be ignored by the device. A maximum of time of “tSUS” (See *AC Characteristics*) is required to suspend the erase/program operation. The BUSY bit in the Status Register will be cleared from 1 to0 within “tSUS” and the SUS bit in the Status Register will be set from 0 to 1 immediately after Erase/Program Suspend. For a previously resumed Erase/Program operation, it is also required that the Suspend instruction “75h” is not issued earlier than a minimum of time of “tSUS” following the preceding Resume instruction “7Ah”.

Unexpected power off during the Erase/Program Suspend state will reset the device and release the suspend state. SUS1 bit or SUS2 bit in the Status Register will also reset to 0. The data within the page, sector or block that was being suspended may become corrupted. It is recommended for the user to implement system design techniques against the accidental power interruption and preserve data integrity during Erase/Program Suspend state.

Figure 7.4.7a. Erase/Program Suspend Instruction (SPI Mode)

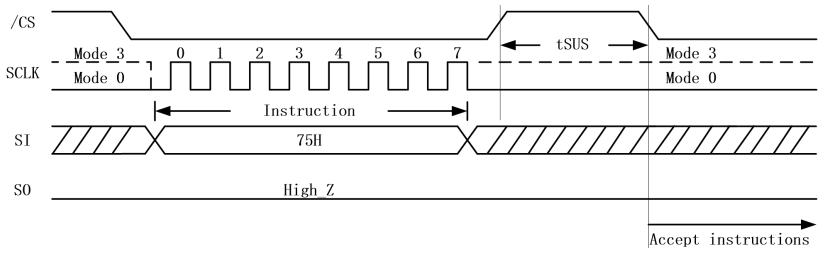
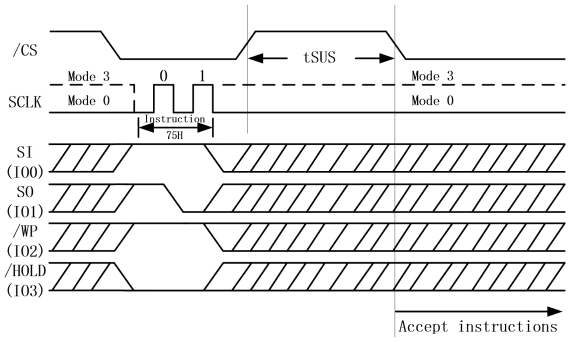


Figure 7.4.7b. Erase/Program Suspend Instruction (QPI Mode)



7.4.8 Erase/Program Resume (7Ah)

The Erase/Program Resume instruction “7Ah” must be written to resume the page program or Sector/Block Erase operation after an Erase/Program Suspend. The Resume instruction “7Ah” will be accepted by the device only if the SUS1 bit or SUS2 bit in the Status Register equals to 1 and the BUSY bit equals to 0. After issued the SUS1 bit or SUS2 bit will be cleared from 1 to 0 immediately, the BUSY bit will be set from 0 to 1 within 200ns and the page or Sector or Block will complete the erase/program operation. If the SUS1 bit or SUS2 bit equals to 0 or the BUSY bit equals to 1, the Resume instruction “7Ah” will be ignored by the device. The Erase/Program Resume instruction sequence is shown in *Figure 7.4.8a* (SPI mode) & *Figure 7.4.8b* (QPI mode).

Resume instruction is ignored if the previous Erase/Program Suspend operation was interrupted by unexpected power off. It is also required that a subsequent Erase/Program Suspend instruction not to be issued within a minimum of time of “tSUS” following a previous Resume instruction.

Figure 7.4.8a. Erase/Program Resume Instruction (SPI Mode)

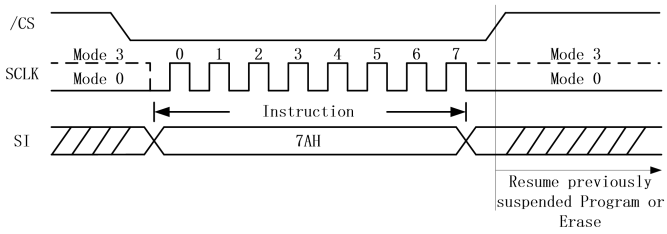
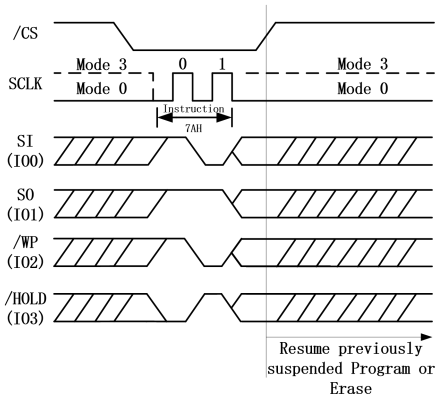


Figure 7.4.8b. Erase/Program Resume Instruction (QPI Mode)



7.4.9 Erase Security Registers (44h)

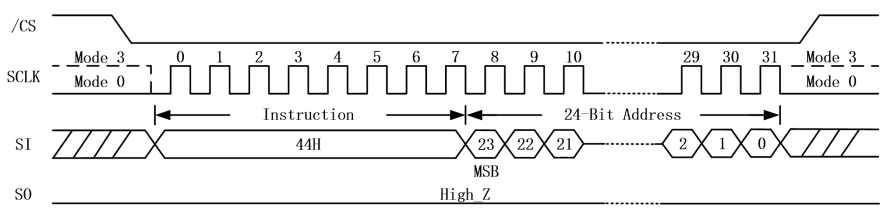
The BY25Q64AL offers three 256-byte Security Registers which can be erased and programmed individually. These registers may be used by the system manufacturers to store security and other important information separately from the main memory array.

The Erase Security Register instruction is similar to the *Sector Erase* instruction. A *Write Enable* instruction must be executed before the device will accept the Erase Security Register Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “44h” followed by a 24-bit address (A23-A0) to erase one of the three security registers.

ADDRESS	A23-16	A15-12	A11-8	A7-0
Security Register #1	00h	0 0 0 1	0 0 0 0	Don’t Care
Security Register #2	00h	0 0 1 0	0 0 0 0	Don’t Care
Security Register #3	00h	0 0 1 1	0 0 0 0	Don’t Care

The Erase Security Register instruction sequence is shown in *Figure 7.4.9*. The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the instruction will not be executed. After /CS is driven high, the self-timed Erase Security Register operation will commence for a time duration of tSE (See *AC Characteristics*). While the Erase Security Register cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Erase Security Register cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Security Register Lock Bits (LB3-1) in the Status Register-2 can be used to OTP protect the security registers. Once a lock bit is set to 1, the corresponding security register will be permanently locked, Erase Security Register instruction to that register will be ignored (Refer to *section 5.4.2.6* and *section 7.1.5* for detail descriptions).

Figure 7.4.9. Erase Security Registers Instruction (SPI Mode only)



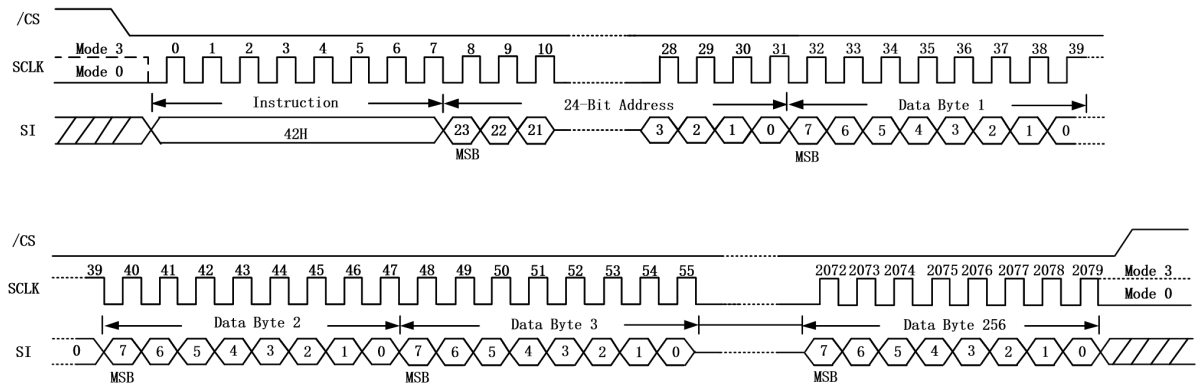
7.4.10 Program Security Registers (42h)

The Program Security Register instruction is similar to the *Page Program* instruction. It allows from one byte to 256 bytes of security register data to be programmed at previously erased (FFh) memory locations. A Write Enable instruction must be executed before the device will accept the Program Security Register Instruction (Status Register bit WEL= 1). The instruction is initiated by driving the /CS pin low then shifting the instruction code “42h” followed by a 24- bit address (A23-A0) and at least one data byte, into the SI pin. The /CS pin must be held low for the entire length of the instruction while data is being sent to the device.

ADDRESS	A23-16	A15-12	A11-8	A7-0
Security Register #1	00h	0 0 0 1	0 0 0 0	Byte Address
Security Register #2	00h	0 0 1 0	0 0 0 0	Byte Address
Security Register #3	00h	0 0 1 1	0 0 0 0	Byte Address

The Program Security Register instruction sequence is shown in *Figure 7.4.10*. The Security Register Lock Bits (LB3-1) in the Status Register-2 can be used to OTP protect the security registers. Once a lock bit is set to 1, the corresponding security register will be permanently locked, Program Security Register instruction to that register will be ignored (See 7.1.8, 8.2.25 for detail descriptions).

Figure 7.4.10. Program Security Registers Instruction (SPI Mode only)

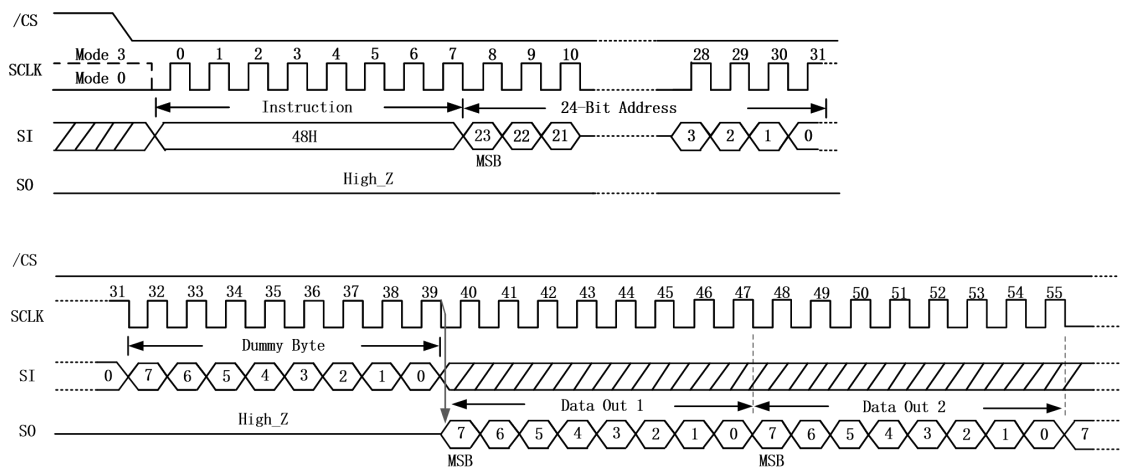


7.4.11 Read Security Registers (48h)

The Read Security Register instruction is similar to the *Fast Read* instruction and allows one or more data bytes to be sequentially read from one of the three security registers. The instruction is initiated by driving the /CS pin low and then shifting the instruction code “48h” followed by a 24-bit address (A23-A0) and eight “dummy” clocks into the SI pin. The code and address bits are latched on the rising edge of the SCLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the SO pin at the falling edge of SCLK with most significant bit (MSB) first. The byte address is automatically incremented to the next byte address after each byte of data is shifted out. Once the byte address reaches the last byte of the register (byte address FFh), it will reset to address 00h, the first byte of the register, and continue to increment. The instruction is completed by driving /CS high. The Read Security Register instruction sequence is shown in *Figure 7.4.11*. If a Read Security Register instruction is issued while an Erase, Program or Write cycle is in process (BUSY=1) the instruction is ignored and will not have any effects on the current cycle. The Read Security Register instruction allows clock rates from D.C. to a maximum of FR (see *AC Electrical Characteristics*).

ADDRESS	A23-16	A15-12	A11-8	A7-0
Security Register #1	00h	0 0 0 1	0 0 0 0	Byte Address
Security Register #2	00h	0 0 1 0	0 0 0 0	Byte Address
Security Register #3	00h	0 0 1 1	0 0 0 0	Byte Address

Figure 7.4.11. Read Security Registers Instruction (SPI Mode only)



7.4.12 Set Read Parameters (C0h)

In QPI mode, to accommodate a wide range of applications with different needs for either maximum read frequency or minimum data access latency, “Set Read Parameters (C0h)” instruction can be used to configure the number of dummy clocks for “*Fast Read (0Bh)*” , “*Fast Read Quad I/O (EBh)*” & “*Burst Read with Wrap (0Ch)*” instructions, and to configure the number of bytes of “Wrap Length” for the “*Burst Read with Wrap (0Ch)*” instruction.

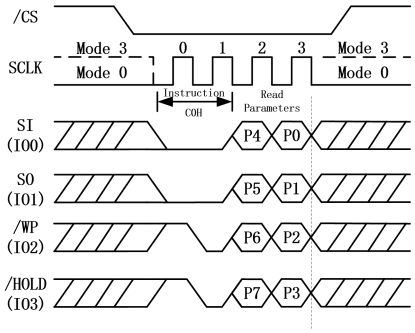
In Standard SPI mode, the “Set Read Parameters (C0h)” instruction is not accepted. The dummy clocks for various Fast Read instructions in Standard/Dual/Quad SPI mode are fixed, please refer to the *Instruction Table 2* for details. The “Wrap Length” is set by W5-4 bit in the “*Set Burst with Wrap (77h)*” instruction. This setting will remain unchanged when the device is switched from Standard SPI mode to QPI mode.

The default “Wrap Length” after a power up or a Reset instruction is 8 bytes, the default number of dummy clocks is 2. The number of dummy clocks is only programmable for “Fast Read (0Bh)”, “Fast Read Quad I/O (EBh)” & “Burst Read with Wrap (0Ch)” instructions in the QPI mode. Whenever the device is switched from SPI mode to QPI mode, the number of dummy clocks and “Wrap Length” should be set again, prior to any 0Bh, EBh or 0Ch instructions.

P5 – P4	DUMMY CLOCKS	MAXIMUM READ FREQ.	MAXIMUM READ FREQ. (A[1:0]=0,0)
0 0	2	33MHz	33MHz
0 1	4	55MHz	80MHz
1 0	6	80MHz	108MHz

P1 – P0	WRAP LENGTH
0 0	8-byte
0 1	16-byte
1 0	32-byte
1 1	64-byte

Figure 7.4.12. Set Read Parameters Instruction (QPI Mode only)



7.4.13 Enter QPI Mode (38h)

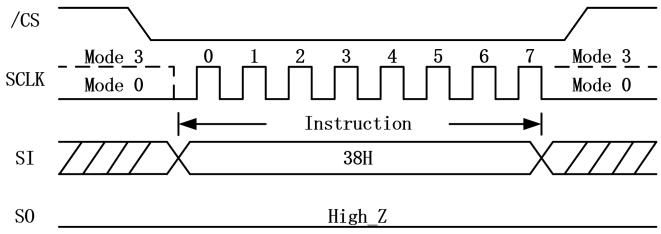
The BY25Q64AL support both Standard/Dual/Quad Serial Peripheral Interface (SPI) and Quad Peripheral Interface (QPI). However, SPI mode and QPI mode cannot be used at the same time. “Enter QPI (38h)” instruction is the only way to switch the device from SPI mode to QPI mode.

Upon power-up, the default state of the device upon is Standard/Dual/Quad SPI mode. This provides full backward compatibility with earlier generations of BY Technology serial flash memories. See *Instruction Set Table 1- 2* for all supported SPI commands. In order to switch the device to QPI mode, the Quad Enable (QE) bit in Status Register-2 must be set to 1 first, and an “Enter QPI (38h)” instruction must be issued. If the Quad Enable (QE) bit is 0, the “Enter QPI (38h)” instruction will be ignored and the device will remain in SPI mode.

See *Instruction Set Table 3* for all the commands supported in QPI mode.

When the device is switched from SPI mode to QPI mode, the existing Write Enable and Erase/Program Suspend status, and the Wrap Length setting will remain unchanged.

Figure 7.4.13. Enter QPI Instruction (SPI Mode only)

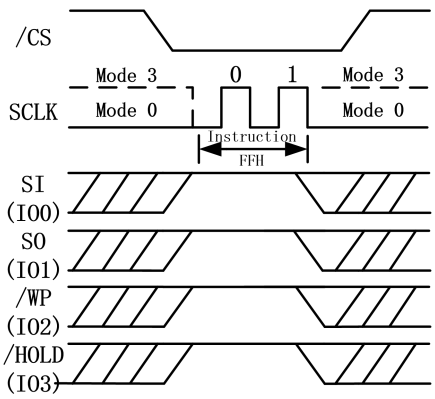


7.4.14 Exit QPI Mode (FFh)

In order to exit the QPI mode and return to the Standard/Dual/Quad SPI mode, an “Exit QPI (FFh)” instruction must be issued.

When the device is switched from QPI mode to SPI mode, the existing Write Enable Latch (WEL) and Erase/Program Suspend status, and the Wrap Length setting will remain unchanged.

Figure 7.4.14. Exit QPI Instruction (QPI Mode only)



7.4.15 Dynamic Protection Block/Sector Lock (36h)

The Dynamic Protection Block/Sector Lock/Unlock provides an alternative way to protect the memory array from adverse Erase/Program. In order to use the Dynamic Protection Block/Sector Lock/Unlock, the WPS bit in Status Register-3 must be set to 1. If WPS=0, the write protection will be determined by the combination of CMP, SEC, TB, BP[2:0] bits in the Status Registers. The Dynamic Protection Block/Sector Lock bits are volatile bits. The default values after device power up or after a Reset are 1, so the entire memory array is being protected.

To lock a specific block or sector as illustrated in *Figure 7.4.15a* (SPI mode) or *Figure 7.4.15b* (QPI mode), an Dynamic Protection Block/Sector Lock command must be issued by driving /CS low, shifting the instruction code “36h” into the Data Input pin on the rising edge of SCLK, followed by a 24-bit address and then driving /CS high. A Write Enable instruction must be executed before the device will accept the Dynamic Protection Block/Sector Lock Instruction (Status Register bit WEL= 1).

Figure 7.4.15a. Dynamic Protection Block/Sector Lock Instruction (SPI Mode)

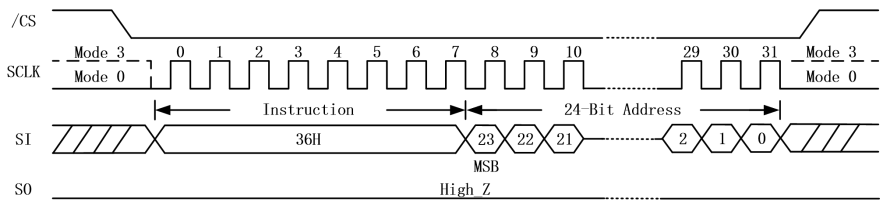
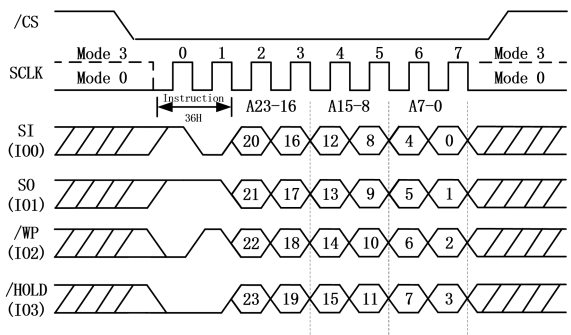


Figure 7.4.15b. Dynamic Protection Block/Sector Lock Instruction (QPI Mode)



7.4.16 Dynamic Protection Block/Sector Unlock (39h)

The Dynamic Protection Block/Sector Lock/Unlock provides an alternative way to protect the memory array from adverse Erase/Program. In order to use the Dynamic Protection Block/Sector Lock/Unlock, the WPS bit in Status Register-3 must be set to 1. If WPS=0, the write protection will be determined by the combination of CMP, SEC, TB, BP[2:0] bits in the Status Registers. The Dynamic Protection Block/Sector Lock bits are volatile bits. The default values after device power up or after a Reset are 1, so the entire memory array is being protected.

To unlock a specific block or sector as illustrated in *Figure 7.4.16a* (SPI mode) or *Figure 7.4.16b* (QPI mode), an Dynamic Protection Block/Sector Unlock command must be issued by driving /CS low, shifting the instruction code “39h” into the Data Input pin on the rising edge of SCLK, followed by a 24- bit address and then driving /CS high. A Write Enable instruction must be executed before the device will accept the Dynamic Protection Block/Sector Unlock Instruction (Status Register bit WEL= 1).

Figure 7.4.16a. Individual Block Unlock Instruction (SPI Mode)

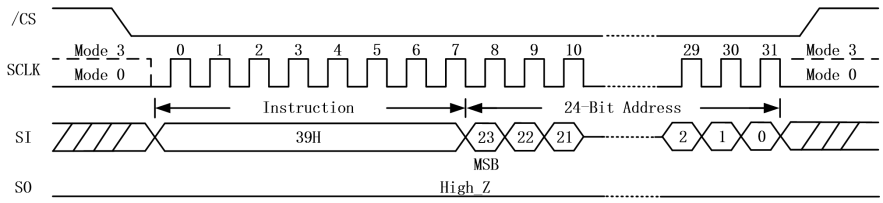
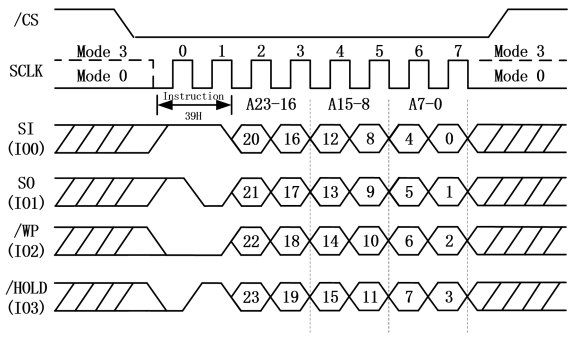


Figure 7.4.16b. Individual Block Unlock Instruction (QPI Mode)



7.4.17 Read Block/Sector Lock (3Dh)

The Dynamic Protection Block/Sector Lock/Unlock provides an alternative way to protect the memory array from adverse Erase/Program. In order to use the Dynamic Protection Block/Sector Lock/Unlock, the WPS bit in Status Register-3 must be set to 1. If WPS=0, the write protection will be determined by the combination of CMP, SEC, TB, BP[2:0] bits in the Status Registers. The Dynamic Protection Block/Sector Lock bits are volatile bits. The default values after device power up or after a Reset are 1, so the entire memory array is being protected.

To read out the lock bit value of a specific block or sector as illustrated in *Figure 7.4.17a* (SPI mode) or *Figure 7.4.17b* (QPI mode), a Read Block/Sector Lock command must be issued by driving /CS low, shifting the instruction code “3Dh” into the Data Input pin on the rising edge of SCLK, followed by a 24-bit address. The Block/Sector Lock bit value will be shifted out on the Data Output pin at the falling edge of SCLK with most significant bit (MSB) first as shown in Figure 7.4.17a and 7.4.17b. If the least significant bit (LSB) is 1, the corresponding block/sector is locked; if LSB=0, the corresponding block/sector is unlocked, Erase/Program operation can be performed.

Figure 7.4.17a. Read Block Lock Instruction (SPI Mode)

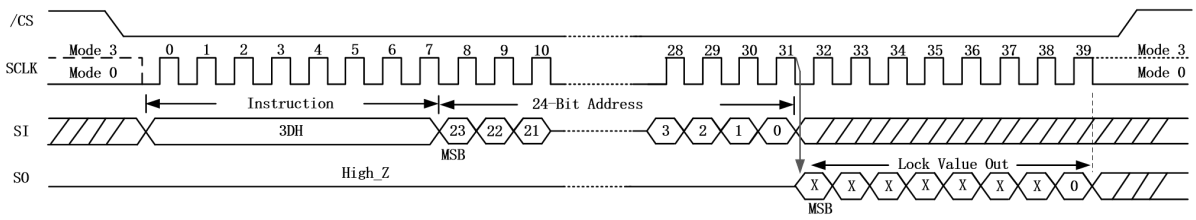
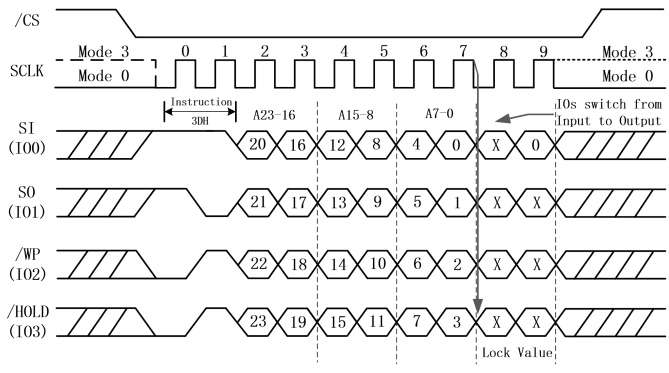


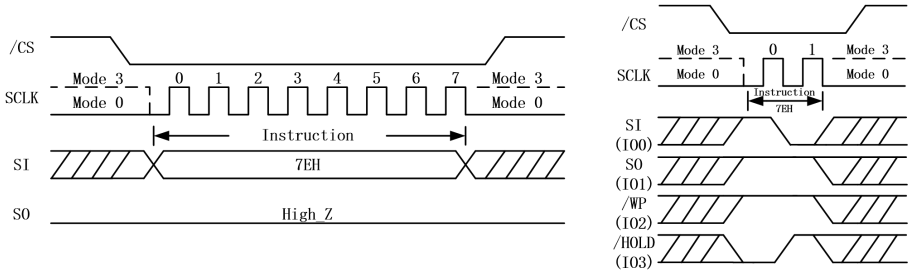
Figure 7.4.17b. Read Block Lock Instruction (QPI Mode)



7.4.18 Global Block/Sector Lock (7Eh)

All Block/Sector Lock bits can be set to 1 by the Global Block/Sector Lock instruction. The command must be issued by driving /CS low, shifting the instruction code “7Eh” into the Data Input pin on the rising edge of SCLK, and then driving /CS high. A Write Enable instruction must be executed before the device will accept the Global Block/Sector Lock Instruction (Status Register bit WEL= 1).

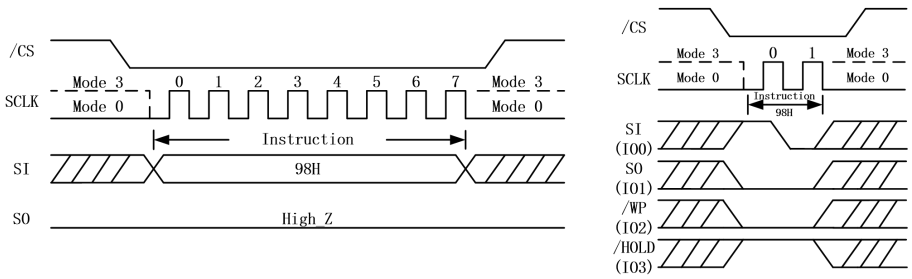
Figure 7.4.18. Global Block Lock Instruction for SPI Mode (left) or QPI Mode (right)



7.4.19 Global Block/Sector Unlock (98h)

All Block/Sector Lock bits can be set to 0 by the Global Block/Sector Unlock instruction. The command must be issued by driving /CS low, shifting the instruction code “98h” into the Data Input pin on the rising edge of SCLK, and then driving /CS high. A Write Enable instruction must be executed before the device will accept the Global Block/Sector Unlock Instruction (Status Register bit WEL= 1).

Figure 7.4.19. Global Block Unlock Instruction for SPI Mode (left) or QPI Mode (right)



7.4.20 Enable Reset (66h) and Reset Device (99h)

Because of the small package and the limitation on the number of pins, the BY25Q64AL provide a software Reset instruction instead of a dedicated RESET pin. Once the Reset instruction is accepted, any on-going internal operations will be terminated and the device will return to its default power-on state and lose all the current volatile settings, such as Volatile Status Register bits, Write Enable Latch (WEL) status, Erase/Program Suspend status, Read parameter setting (P7-P0), Continuous Read Mode bit setting (M7-M0) , Wrap Bit setting (W6-W4) and the Dynamic Protection Block/Sector Lock bits.

“ Enable Reset (66h)” and “Reset (99h)” instructions can be issued in either SPI mode or QPI mode. To avoid accidental reset, both instructions must be issued in sequence. Any other commands other than “Reset (99h)” after the “Enable Reset (66h)” command will disable the “Reset Enable” state. A new sequence of “Enable Reset (66h)” and “Reset (99h)” is needed to reset the device. Once the Reset command is accepted by the device, the device will take approximately tRST=30us to reset. During this period, no command will be accepted.

Data corruption may happen if there is an on-going or suspended internal Erase or Program operation when Reset command sequence is accepted by the device. It is recommended to check the BUSY bit and the SUS bit in Status Register before issuing the Reset command sequence.

Figure 7.4.20a. Enable Reset and Reset Instruction Sequence (SPI Mode)

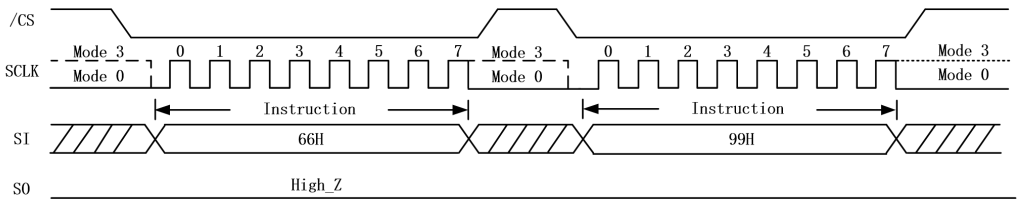
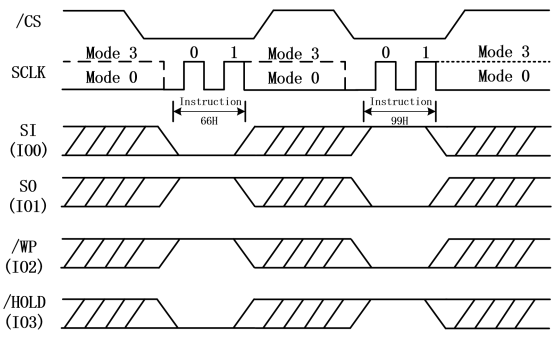


Figure 7.4.20b. Enable Reset and Reset Instruction Sequence (QPI Mode)



7.4.21 JEDEC Standard Hardware Reset

The Exit Ultra-Deep Power-Down / Hardware Reset command sequence can be wakeup the device from Ultra-Deep Power-Down. The sequence can also be used to reset the device to its power on state without cycling power. It is in any case recommended to run a Hardware reset command sequence after every time the device is powered up.

The reset sequence does not use the SCK pin. The SCK has to be low (mode 0) or high (mode 3) through the entire reset sequence. This prevents any confusion with a command, as no command bits are transferred (clocked).

A reset is commanded when the data on the SI pin is 0101 on four consecutive positive edges of the /CS pin with no edge on the SCK pin throughout. The is a sequence where

1) /CS is driven active low to select the device.

2) Clock (SCK) remains stable in either a high or low state.

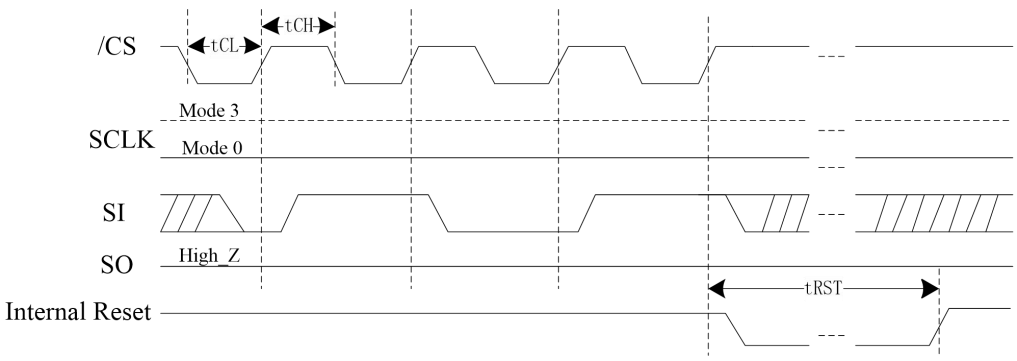
3) SI is driven low by the bus master, simultaneously with /CS going active low. No SPI bus slave drives SI during /CS low before a transition of SCK i.e.: slave streaming output active is not allowed until after the first edge of SCK.

4) /CS is driven inactive. The slave captures the state of SI on the rising edge of /CS

The above steps are repeated 4 time, each time alternating the state of SI.

After the fourth /CS pulse, the slave triggers its internal reset. SI is low on the first /CS, high on the second, low on the third, high on the fourth. This provides a value of 5H, unlike random noise. Any activity on SCK during this time will halt the sequence and a Reset will not be generated. Figure below illustrates the timing for hardware Reset operation.

Figure 7.4.21. JEDEC Standard Hardware Reset



Parameter	Min.	Typ.	Max.	Unit.
tCL	20			ns
tCH	20			ns
Setup Time	5			ns
Hold Time	5			ns

7.4.22 Read Serial Flash Discoverable Parameter (5AH)

The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. The concept is similar to the one found in the Introduction of JEDEC Standard, JESD68 on CFI.SFDP is a standard of JEDEC Standard No.216.

Figure 7.4.22a. Read Serial Flash Discoverable Parameter command Sequence Diagram(SPI Mode)

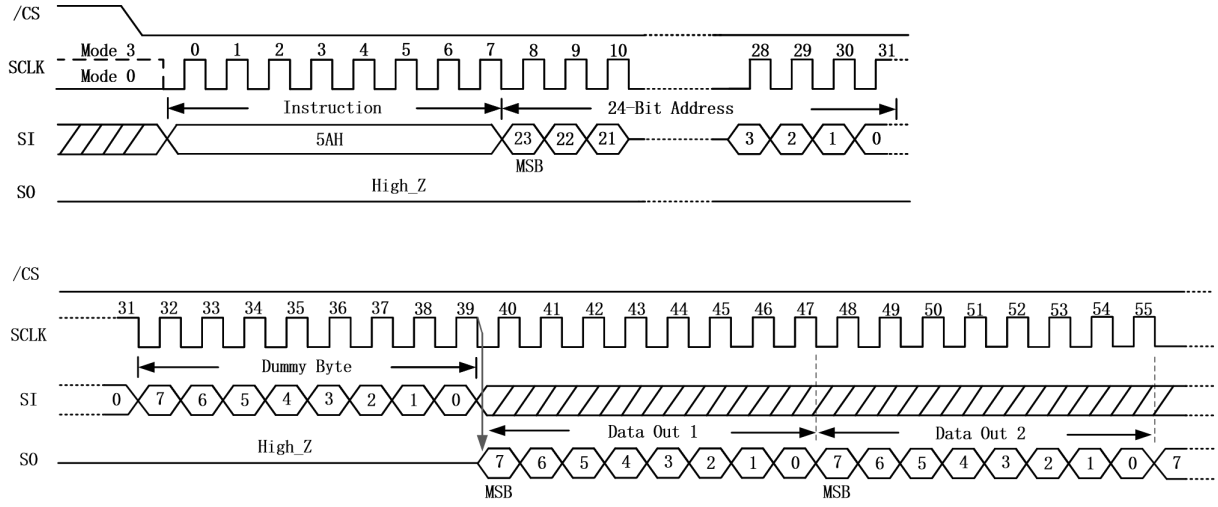


Figure 7.4.22b. Read Serial Flash Discoverable Parameter command Sequence Diagram(QPI Mode)

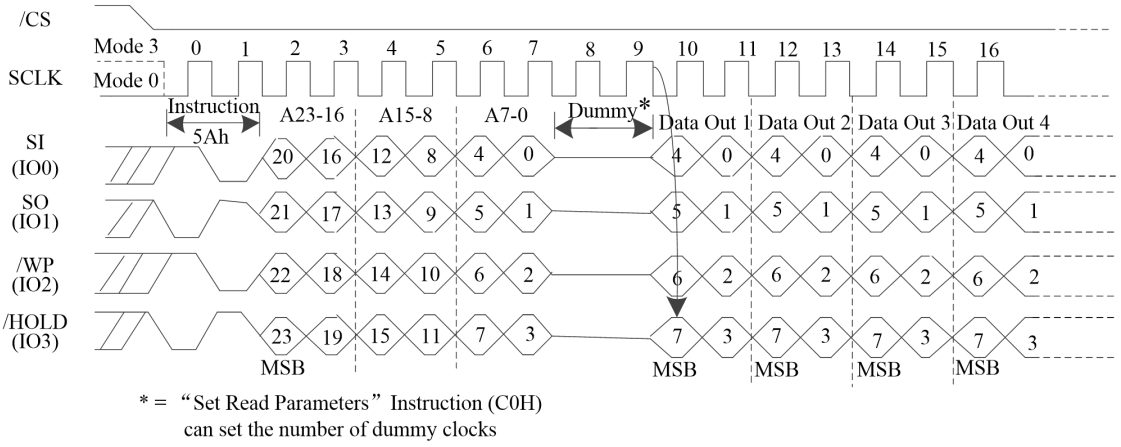


Table 14. Signature and Parameter Identification Data Values

Description	Comment	Add(H) (Byte)	DW Add (Bit)	Data	Data
SFDP Signature	Fixed:50444653H	00H	07:00	53H	53H
		01H	15:08	46H	46H
		02H	23:16	44H	44H
		03H	31:24:	50H	50H
SFDP Minor Revision Number	Start from 00H	04H	07:00	00H	00H
SFDP Major Revision Number	Start from 01H	05H	15:08	01H	01H
Number of Parameters Headers	Start from 00H	06H	23:16	01 H	01 H
Unused	Contains 0xFFH and can never be changed	07H	31:24	FFH	FFH
ID number (JEDEC)	00H: It indicates a JEDEC specified header	08H	07:00	00H	00H
Parameter Table Minor Revision Number	Start from 0x00H	09H	15:08	00H	00H
Parameter Table Major Revision Number	Start from 0x01H	0AH	23:16	01H	01H
Parameter Table Length (in double word)	How many DWORDs in the Parameter table	0BH	31:24	09H	09H
Parameter Table Pointer (PTP)	First address of JEDEC Flash Parameter table	0CH	07:00	30H	30H
		0DH	15:08	00H	00H
		0EH	23:16	00H	00H
Unused	Contains 0xFFH and can never be changed	0FH	31:24	FFH	FFH
ID Number LSB (Manufacturer ID)	It is indicates BY Technology Device manufacturer ID	10H	07:00	68H	68H
Parameter Table Minor Revision Number	Start from 0x00H	11 H	15:08	00H	00H
Parameter Table Major Revision Number	Start from 0x01H	12H	23:16	01H	01H
Parameter Table Length (in double word)	How many DWORDs in the Parameter table	13H	31:24	03H	03H
Parameter Table Pointer (PTP)	First address of BY Technology Device Flash Parameter table	14H	07:00	60H	60H
		15H	15:08	00H	00H
		16H	23:16	00H	00H
Unused	Contains 0xFFH and can never be changed	17H	31:24	FFH	FFH

Table 15. Parameter Table (0): JEDEC Flash Parameter Tables

Description	Comment	Add(H) (Byte)	DW Add (Bit)	Data	Data
Block/Sector Erase Size	00: Reserved; 01: 4KB erase; 10: Reserved; 11: not support 4KB erase	30H	01:00	01b	E5H
Write Granularity	0: 1Byte, 1: 64Byte or larger		02	1b	
Write Enable Instruction Requested for Writing to Volatile Status Registers	0: Nonvolatile status bit 1: Volatile status bit (BP status register bit)		03	0b	
Write Enable Opcode Select for Writing to Volatile Status Registers	0: Use 50H Opcode, 1: Use 06H Opcode, Note: If target flash status register is Nonvolatile, then bits 3 and 4 must be set to 00b.		04	0b	
Unused	Contains 111b and can never be changed		07:05	111b	
4KB Erase Opcode		31H	15:08	20H	20H
(1 -1 -2) Fast Read	0=Not support, 1=Support	32H	16	1b	F1H
Address Bytes Number used in addressing flash array	00: 3Byte only, 01: 3 or 4Byte, 10: 4Byte only, 11: Reserved		18:17	00b	
Double Transfer Rate (DTR) clocking	0=Not support, 1=Support		19	0b	
(1 -2-2) Fast Read	0=Not support, 1=Support		20	1b	
(1 -4-4) Fast Read	0=Not support, 1=Support		21	1b	
(1 -1 -4) Fast Read	0=Not support, 1=Support		22	1b	
Unused			23	1b	
Unused		33H	31:24	FFH	FFH
Flash Memory Density		37H:34	31:00	07FFFFFFH	
(1 -4-4) Fast Read Number of Wait states	00000b: Wait states (Dummy Clocks) not support	38H	04:00	00100b	44H
(1 -4-4) Fast Read Number of Mode Bits	000b:Mode Bits not support		07:05	010b	
(1 -4-4) Fast Read Opcode		39H	15:08	EBH	EBH
(1 -1 -4) Fast Read Number of Wait states	00000b: Wait states (Dummy Clocks) not support	3AH	20:16	01000b	08H
(1 -1 -4) Fast Read Number of Mode Bits	000b:Mode Bits not support		23:21	000b	
(1 -1 -4) Fast Read Opcode		3BH	31:24	6BH	6BH
(1 -1 -2) Fast Read Number of Wait states	00000b: Wait states (Dummy Clocks) not support	3CH	04:00	01000b	08H
(1 -1 -2) Fast Read Number of Mode Bits	000b: Mode Bits not support		07:05	000b	
(1 -1 -2) Fast Read Opcode		3DH	15:08	3BH	3BH
(1 -2-2) Fast Read Number of Wait states	0000b: Wait states (Dummy Clocks) not support	3EH	20:16	00010b	42H
(1 -2-2) Fast Read Number of Mode Bits	000b: Mode Bits not support		23:21	010b	
(1 -2-2) Fast Read Opcode		3FH	31:24	BBH	BBH
(2-2-2) Fast Read	0=not support 1=support	40H	00	0b	FEH
Unused			03:01	111b	
(4-4-4) Fast Read	0=not support 1=support		04	1b	
Unused			07:05	111b	
Unused		43H:41H	31:08	0xFFH	0xFFH
Unused		45H:44H	15:00	0xFF	0xFFH

				H	
(2-2-2) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support	46H	20:16	00000b	00H
(2-2-2) Fast Read Number of Mode Bits	000b: Mode Bits not support		23:21	000b	
(2-2-2) Fast Read Opcode		47H	31:24	FFH	FFH
Unused		49H:48H	15:00	0xFFH	0xFFH
(4-4-4) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support	4AH	20:16	00100b	44H
(4-4-4) Fast Read Number of Mode Bits	000b: Mode Bits not support		23:21	010b	
(4-4-4) Fast Read Opcode		4BH	31:24	EBH	EBH
Sector Type 1 Size	Sector/block size=2^N bytes 0x00b: this sector type don't exist	4CH	07:00	0CH	0CH
Sector Type 1 erase Opcode		4DH	15:08	20H	20H
Sector Type 2 Size	Sector/block size=2^N bytes 0x00b: this sector type don't exist	4EH	23:16	0FH	0FH
Sector Type 2 erase Opcode		4FH	31:24	52H	52H
Sector Type 3 Size	Sector/block size=2^N bytes 0x00b: this sector type don't exist	50H	07:00	10H	10H
Sector Type 3 erase Opcode		51H	15:08	D8H	D8H
Sector Type 4 Size	Sector/block size=2^N bytes 0x00b: this sector type don't exist	52H	23:16	00H	00H
Sector Type 4 erase Opcode		53H	31:24	FFH	FFH

Table 16. Parameter Table (1): BY Technology Device Flash Parameter Tables

Description	Comment	Add(H) (Byte)	DW Add (Bit)	Data	Data
Vcc Supply Maximum Voltage	2000H=2.000V 2700H=2.700V 3600H=3.600V	61H:60H	15:00	2000H	2000H
Vcc Supply Minimum Voltage	1650H=1.650V 2250H=2.250V 2350H=2.350V 2700H=2.700V	63H:62H	31:16	1650H	1650H
HW Reset# pin	0=not support 1=support	65H:64H	00	1b	F99FH
HW Hold# pin	0=not support 1=support		01	1b	
Deep Power Down Mode	0=not support 1=support		02	1b	
SW Reset	0=not support 1=support		03	1b	
SW Reset Opcode	Should be issue Reset Enable(66H)before Reset cmd.		11:04	99H	
Program Suspend/Resume	0=not support 1=support		12	1b	
Erase Suspend/Resume	0=not support 1=support		13	1b	
Unused			14	1b	
Wrap-Around Read mode	0=not support 1=support		15	1b	
Wrap-Around Read mode Opcode		66H	23:16	77H	77H
Wrap-Around Read data length	08H:support 8B wrap-around read 16H:8B&16B 32H:8B&16B&32B 64H:8B&16B&32B&64B	67H	31:24	64H	64H
Individual block lock	0=not support 1=support	6BH:68H	00	1b	F8D9H
Individual block lock bit(Volatile/Nonvolatile)	0=Volatile 1=Nonvolatile		01	0b	
Individual block lock Opcode			09:02	36H	
Individual block lock Volatile protect bit default protect status	0=protect 1=unprotect		10	0b	
Secured OTP	0=not support 1=support		11	1b	
Read Lock	0=not support 1=support		12	1b	
Permanent Lock	0=not support 1=support		13	1b	
Unused			15:14	11b	
Unused			31:16	FFFFH	FFFFH

8. Electrical Characteristics

8.1 Absolute Maximum Ratings

PARAMETERS	SYMBOL	CONDITIONS	RANGE	UNIT
Supply Voltage	VCC		–0.6 to VCC+0.6	V
Voltage Applied to Any Pin	VIO	Relative to Ground	–0.6 to VCC+0.6	V
Transient Voltage on any Pin	VIOT	<20nS Transient Relative to Ground	–1.0V to VCC+1.0V	V
Storage Temperature	TSTG		–65 to +150	°C
Lead Temperature	TLEAD		See Note (2)	°C
Electrostatic Discharge Voltage	VESD	Human Body Model(3)	–2000 to +2000	V

Notes:

1. This device has been designed and tested for the specified operation ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may affect device reliability. Exposure beyond absolute maximum ratings may cause permanent damage.
2. Compliant with JEDEC Standard J-STD-20C for small body Sn-Pb or Pb-free (Green) assembly and the European directive on restrictions on hazardous substances (RoHS) 2002/95/EU.
3. JEDEC Std JESD22-A114A (C1=100pF, R1=1500 ohms, R2=500 ohms)

8.2 Operating Ranges

PARAMETER	SYMBOL	CONDITIONS	SPEC		UNIT
			MIN	MAX	
Supply Voltage(1)	VCC	FR = 108MHz, fR = 50MHz	1.65	1.95	V
Ambient Temperature (Operating)	TA	Industrial	–40	+85	°C

Note:

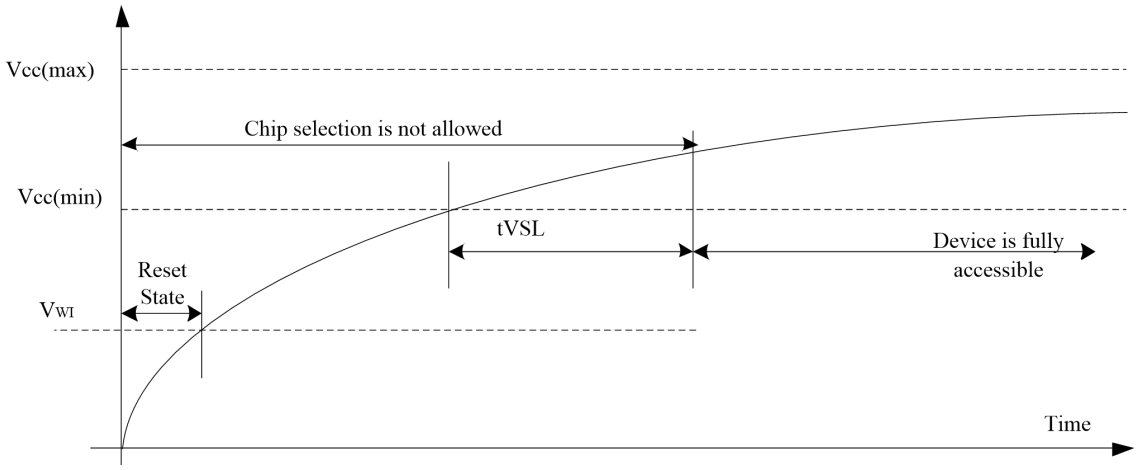
1. VCC voltage during Read can operate across the min and max range but should not exceed ±10% of the programming (erase/write) voltage.

8.3 Power-up Timing and Write Inhibit Threshold

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
VCC(min) to /CS Low	tVSL	300		μs
Write Inhibit Threshold Voltage	Vwi	1.0	1.4	V

Note:

1. These parameters are characterized only.



8.4 DC Electrical Characteristics

PARAMETER	SYMBOL	CONDITIONS	SPEC			UNIT
			MIN	TYP	MAX	
Input Capacitance	CIN(1)	VIN = 0V(1)			6	pF
Output Capacitance	Cout(1)	VOUT = 0V(1)			8	pF
Input Leakage	ILI				±2	µA
I/O Leakage	ILO				±2	µA
Standby Current	ICC1	/CS = VCC, VIN = GND or VCC		10	50	µA
Power-down Current	ICC2	/CS = VCC, VIN = GND or VCC		1	5	µA
Current Read Data / Dual /Quad 1MHz(2)	ICC3	C = 0.1 VCC / 0.9 VCC DO = Open		4	10	mA
Current Read Data / Dual /Quad 50MHz(2)	ICC3	C = 0.1 VCC / 0.9 VCC DO = Open			15	mA
Current Read Data / Dual /Quad 80MHz(2)	ICC3	C = 0.1 VCC / 0.9 VCC DO = Open			18	mA
Current Read Data / Dual Output Read/Quad Output Read 108MHz(2)	ICC3	C = 0.1 VCC / 0.9 VCC DO = Open			20	mA
Current Write Status Register	ICC4	/CS = VCC		8	12	mA
Current Page Program	ICC5	/CS = VCC		20	25	mA
Current Sector/Block Erase	ICC6	/CS = VCC		20	25	mA
Current Chip Erase	ICC7	/CS = VCC		20	25	mA
Input Low Voltage	VIL		–0.5		VCC x 0.3	V
Input High Voltage	VIH		VCC x 0.7		VCC + 0.4	V
Output Low Voltage	VOL	IOL = 100 µA			0.2	V
Output High Voltage	VOH	IOH = –100 µA	VCC – 0.2			V

Notes:

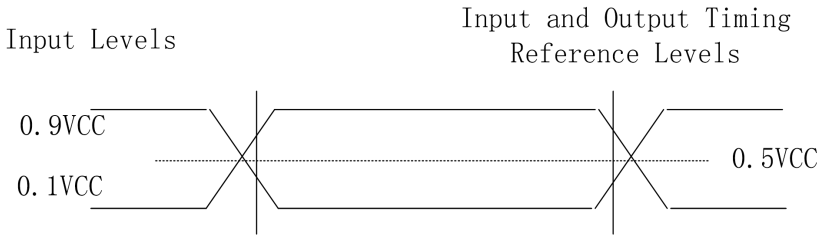
1. Tested on sample basis and specified through design and characterization data. TA = 25° C, VCC = 1.8V.
2. Checker Board Pattern.

8.5 AC Measurement Conditions

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
Load Capacitance	CL		30	pF
Input Rise and Fall Times	TR, TF		5	ns
Input Pulse Voltages	VIN	0.1 VCC to 0.9 VCC		V
Input Timing Reference Voltages	IN	0.3 VCC to 0.7 VCC		V
Output Timing Reference Voltages	OUT	0.5 VCC to 0.5 VCC		V

Note:

1. Output Hi-Z is defined as the point where data out is no longer driven.



8.6 AC Electrical Characteristics

DESCRIPTION	SYMBOL	ALT	SPEC			UNIT
			MIN	TYP	MAX	
Clock frequency for Read Data instruction (03h)	fR		D.C.		50	MHz
Clock frequency for QPI Read instructions (0Bh, EBh, 0Ch), with different dummy clocks	FR	fC1	D.C.		33~108	MHz
Clock frequency for all other SPI/QPI instructions	FR	fC1	D.C.		108	MHz
Clock High, Low Time for all instructions except for Read Data (03h)	tCLH, tCLL(1)		4			ns
Clock High, Low Time for Read Data (03h) instruction	tCRLH, tCRLL(1)		8			ns
Clock Rise Time peak to peak	tCLCH(2)		0.1			V/ns
Clock Fall Time peak to peak	tCHCL(2)		0.1			V/ns
/CS Active Setup Time relative to CLK	tSLCH	tCSS	5			ns
/CS Not Active Hold Time relative to CLK	tCHSL		5			ns
Data In Setup Time	tDVCH	tDSU	2			ns
Data In Hold Time	tCHDX	tDH	3			ns
/CS Active Hold Time relative to CLK	tCHSH		3			ns
/CS Not Active Setup Time relative to CLK	tSHCH		3			ns
/CS Deselect Time (for Array Read Array Read)	tSHSL1	tCSH	10			ns
/CS Deselect Time (for Erase or Program Read Status Registers) Volatile Status Register Write Time	tSHSL2	tCSH	50 50			ns
Output Disable Time	tSHQZ(2)	tDIS			7	ns
Clock Low to Output Valid	tCLQV1	tV1			7	ns
Clock Low to Output Valid (Non-array Read)	tCLQV2	tV2			7.5	ns
Output Hold Time	tCLQX	tHO	2			ns
/HOLD Active Setup Time relative to CLK	tHLCH		5			ns

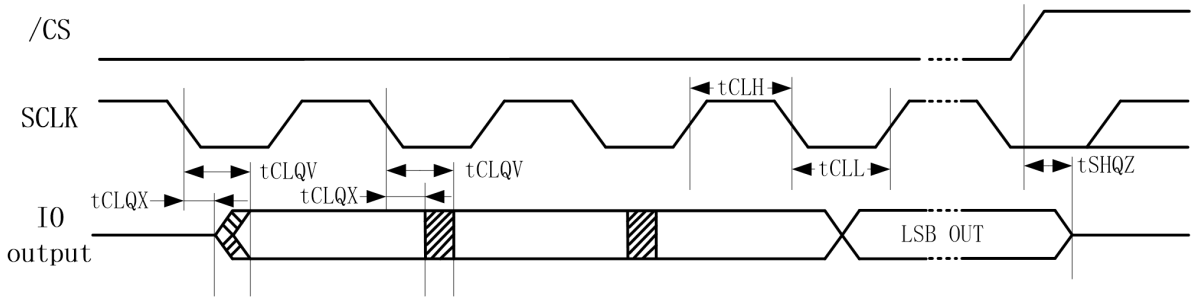
8.7 AC Electrical Characteristics (cont'd)

DESCRIPTION	SYMBOL	ALT	SPEC			UNIT
			MIN	TYP	MAX	
/HOLD Active Hold Time relative to CLK	tCHHH		5			ns
/HOLD Not Active Setup Time relative to CLK	tHHCH	fC1	5			ns
/HOLD Not Active Hold Time relative to CLK	tCHHL	fC1	5			ns
/HOLD to Output Low-Z	tHHQX(2)	tLZ			7	ns
/HOLD to Output High-Z	tHLQZ(2)	tHZ			12	ns
Write Protect Setup Time Before /CS Low	tWHSL(3)		20			ns
Write Protect Hold Time After /CS High	tSHWL(3)		100			ns
/CS High to Power-down Mode	tDP(2)				3	µs
/CS High to Standby Mode without ID Read	tRES1(2)				3	µs
/CS High to Standby Mode with ID Read	tRES2(2)				1.8	µs
/CS High to next Instruction after Suspend	tSUS(2)				60	µs
/CS High to next Instruction after Reset	tRST(2)				30	µs
/RESET pin Low period to reset the device	tRESET(2)		1(5)			µs
Write Status Register Time	tW			5	15	ms
Byte Program Time (First Byte) (4)	tBP1			30	50	µs
Additional Byte Program Time (After First Byte) (4)	tBP2			2.5	12	µs
Page Program Time	tPP			0.7	3	ms
Sector Erase Time (4KB)	tSE			60	300	ms
Block Erase Time (32KB)	tBE1			300	800	ms
Block Erase Time (64KB)	tBE2			500	1200	ms
Chip Erase Time	tCE			30	60	s

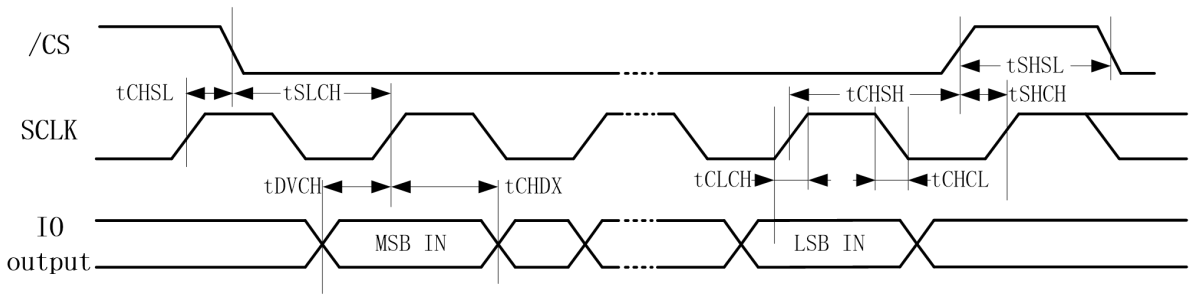
Notes:

1. Clock high + Clock low must be less than or equal to 1/fC.
2. Value guaranteed by design and/or characterization, not 100% tested in production.
3. Only applicable as a constraint for a Write Status Register instruction when SRP[1:0]=(0,1).
4. For multiple bytes after first byte within a page, tBPN = tBP1 + tBP2 * N (typical) and tBPN = tBP1 + tBP2 * N (max), where N = number of bytes programmed.
5. It is possible to reset the device with shorter tRESET (as short as a few hundred ns), a 1us minimum is recommended to ensure reliable operation.
6. Tested on sample basis and specified through design and characterization data. TA = 25° C, VCC = 1.8V, 100% driver strength.

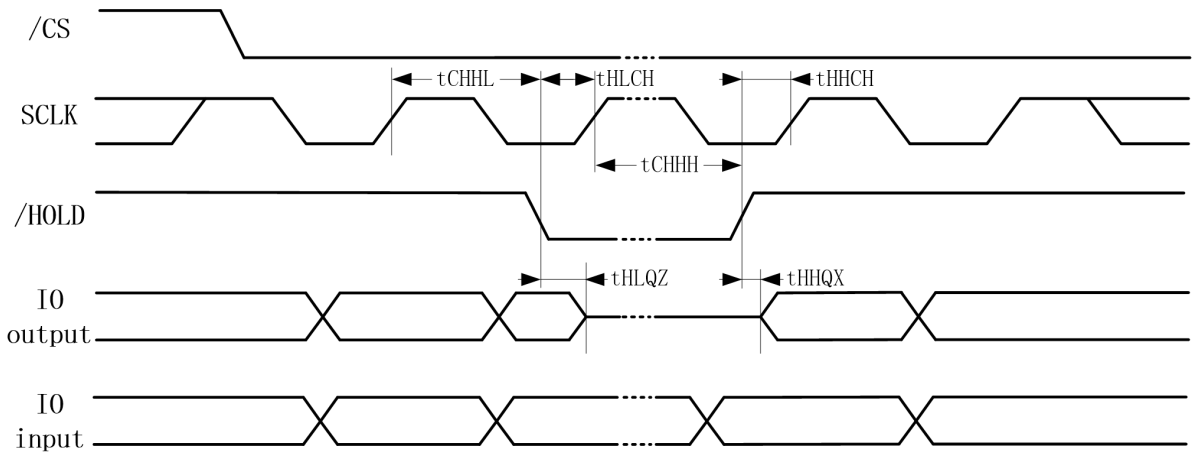
8.8 Serial Output Timing



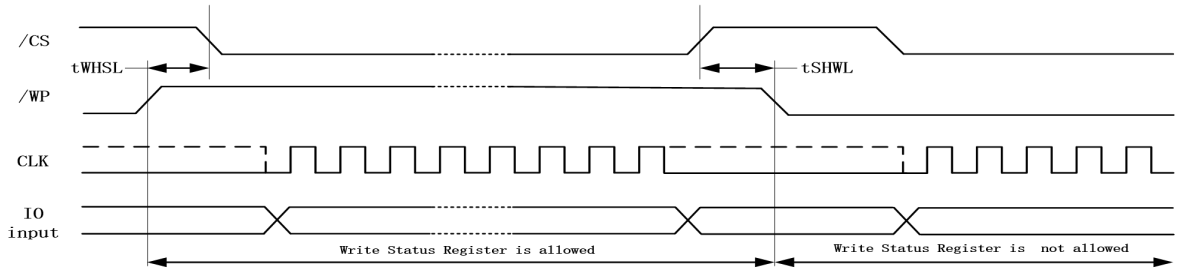
8.9 Serial Input Timing



8.10 /HOLD Timing

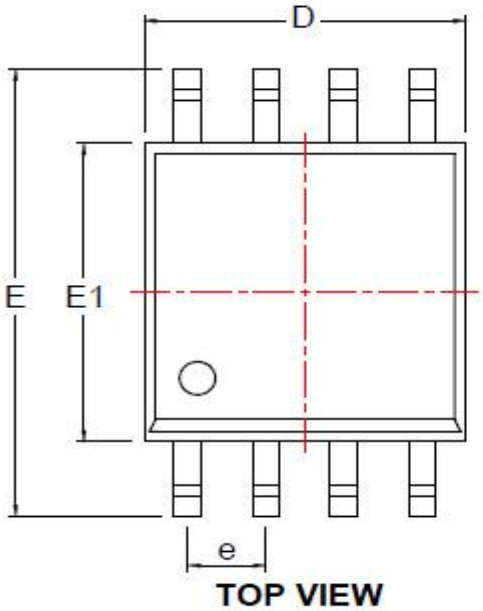


8.11 /WP Timing

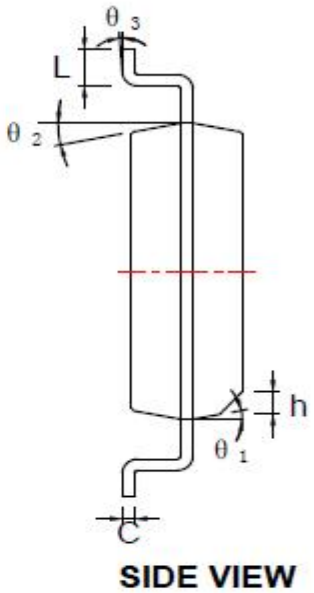


9. Package Information

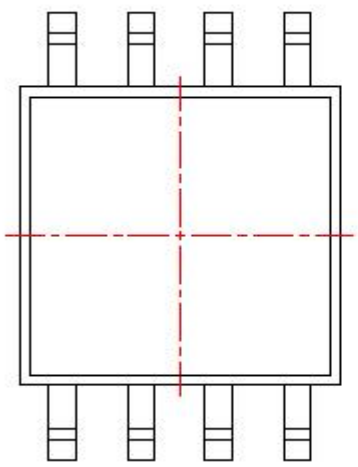
9.1 Package 8-Pin SOP8 208-mil



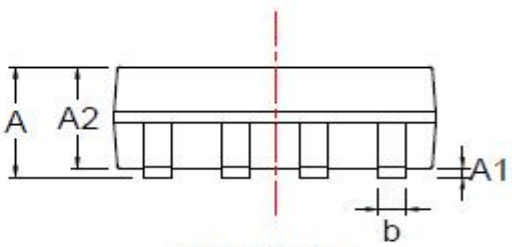
TOP VIEW



SIDE VIEW



BTM VIEW

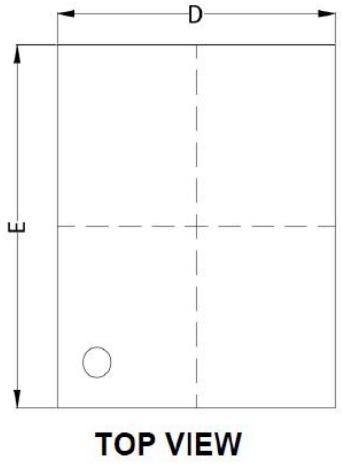


SIDE VIEW

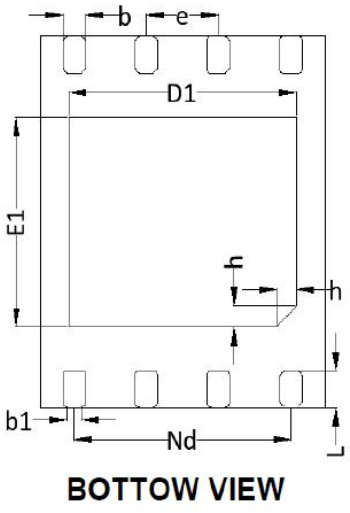
Dimensions

Symbol / Unit		A	A1	A2	b	C	D	E	E1	e	L	h
mm	Min	1.75	0.05	1.70	0.40	0.19	5.13	7.70	5.10	1.27	0.50	0.30
	Nom	1.95	0.15	1.80	0.45	0.20	5.23	7.90	5.25	1.27	0.65	0.40
	Max	2.15	0.25	1.90	0.50	0.21	5.33	8.10	5.40	1.27	0.80	0.50

9.2 Package 8-Pad WSON (6x5mm)



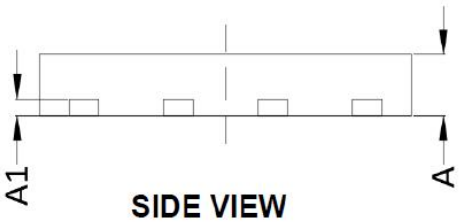
TOP VIEW



BOTTOW VIEW

COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MILLMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1		0.203 REF	
b	0.35	0.40	0.45
b1		0.25 REF	
D	4.90	5.00	5.10
D1	3.90	4.00	4.10
e		1.27BSC	
Nd		3.81BSC	
E	5.90	6.00	6.10
E1	3.30	3.40	3.50
L	0.55	0.60	0.65
h	0.30	0.35	0.40



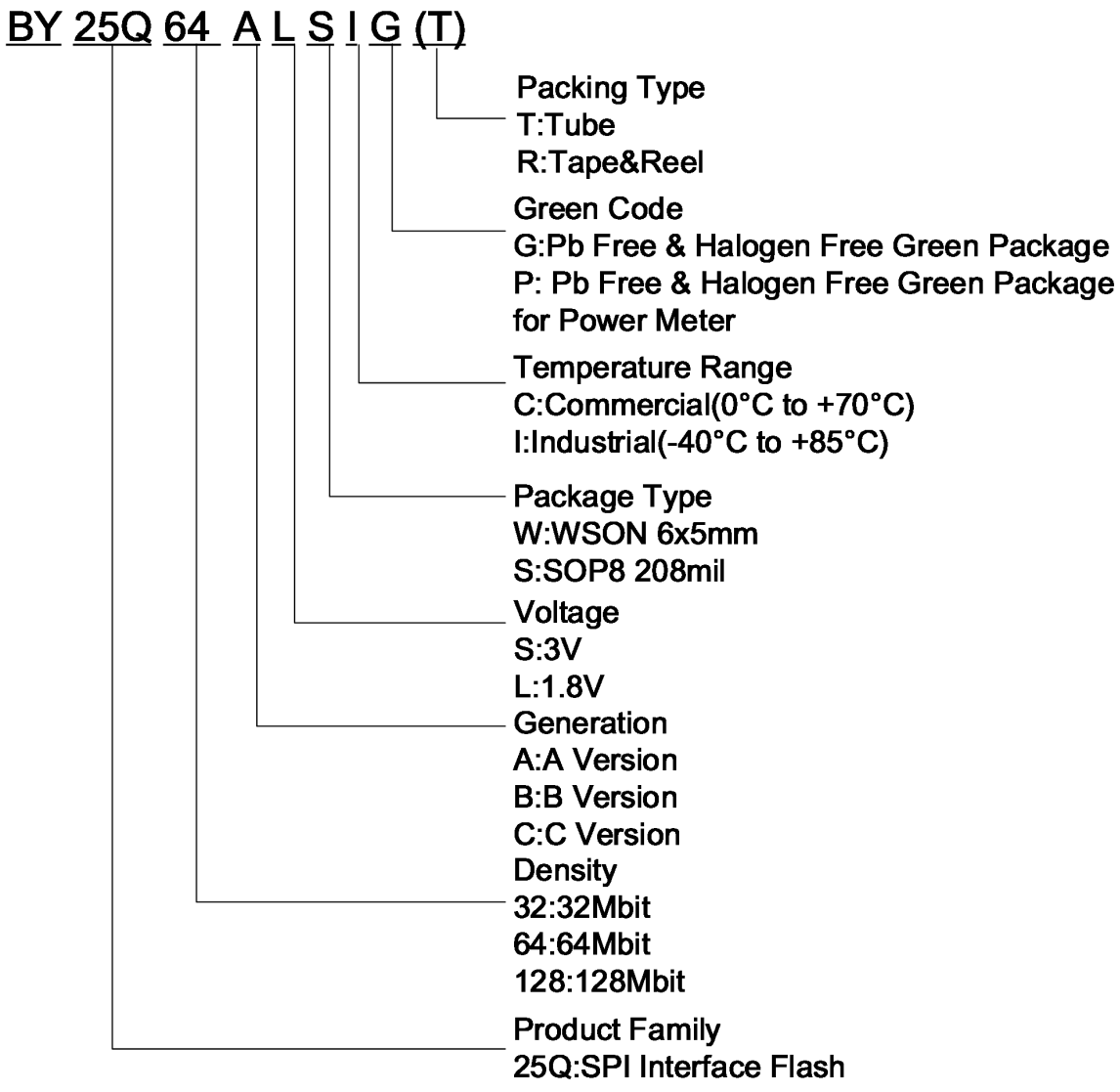
SIDE VIEW

Dimensions

Symbol / Unit		A	A1	b	D	D1	E	E1	e	Nd	L	h
mm	Min	0.70	0.203REF	0.35	4.90	3.9	5.90	3.30	1.27BSC	0.381BSC	0.55	0.30
	Nom	0.75		0.40	5.00	4.0	6.00	3.40			0.60	0.35
	Max	0.80		0.45	5.10	4.1	6.10	3.50			0.65	0.40

Note:
1、The exposed metal pad area on the bottom of the package is floating.

10. Order Information



10.1 Valid part Numbers

The following table provides the valid part numbers for BY25Q64AL SPI Flash Memory. Pls contact BY Technology for specific availability by density and package type.

(T= -40℃~85℃, VCC=1.65~1.95V)

Package Type	Density	Product Number
S SOP8 208mil	64M-bit	BY25Q64ALSIG
W WSON8 6X5mm	64M-bit	BY25Q64ALWIG

10.2 Minimum Packing Quantity (MPQ)

Package Type	Packing Type	Qty for 1 Tube or Reel	Vacuum bag/ Inner Box	MPQ
SOP8 208mil	Tube	95ea/Tube	100Tubes/Bag 1Bag/InnerBox	9,500
	Tape&Reel (13inch, 16mm)	2000ea/Reel	1Reel/Bag 2Bags/InnerBox	4,000
WSON8 6X5mm	Tape&Reel (13inch)	3000ea/Reel	1Reel/Bag 1Bag/InnerBox	3,000

11. Document Change History

REVISION	DATE	ORIGINATOR	DESCRIPTION
1.0	2021-7-1	Zuohuan Yu	Initiate; Base on BY25Q128BL_V2.0;
1.1	2023-4-6	Zuohuan Yu	Update the logo and abbreviation
1.2	2023-07-20	Zuohuan Yu	Add the note of the DFN package