DATASHEET

FOR

1G BIT SPI NOR FLASH

BY25QM1G1FS

Features

- **Serial Peripheral Interface**
  - 4×256M-bit Serial MCP Flash memory
  - Extended SPI: SCLK, /CS, SI, SO, /WP, /HOLD
  - Dual I/O: SCLK, /CS, IO0, IO1 /WP, /HOLD
  - Quad I/O SCLK, /CS, IO0, IO1, IO2, IO3
  - DTR (Double Transfer Rate) Read
  - 3-Byte or 4-Byte Addressing Mode
- **Read**
  - Normal Read (Serial): 108MHz (MAX) clock rate supported for all protocols
  - Double transfer rate Read (DTR): 54MHz (MAX) clock rate supported for all protocols
  - Dual/Quad I/O data transfer up to 216/432 Mbits/S
  - Allows XIP (execute in place) Operation: Continuous Read with16/32/64-byte Wrap
  - Software Reset
- **Program**
  - Serial-input Page Program up to 256 bytes
  - Program Suspend and Resume
- **Erase**
  - Subsector Erase (4 KB)
  - Sector Erase (64 KB)
  - Die Erase (265 MB)
  - Erase Suspend and Resume
- **Program/Erase Speed**
  - Page Program time: 0.5ms typical
  - Subsector Erase time: 250ms typical
  - Sector Erase time: 0.7s typical
  - Die Erase time: 240s typical
- **Flexible Architecture**
  - Subsector of 4K-byte
  - Sector of 64K-byte
- **Low Power Consumption**
  - 20mA maximum active current
  - 200uA maximum Standby current
- **Software/Hardware Write Protection**
  - -Top/Bottom, Complement array protection, protected area size defined by five nonvolatile bits (BP0, BP1, BP2, BP3, and BP4)
  - Software write protection applicable to every 64KB sector via volatile lock bit
  - Enable/Disable protection with /WP Pin
- **Single Supply Voltage**
  - Full voltage range: 2.7~3.6V
- **Temperature Range**
  - Commercial (-40℃ to +85℃)
  - Industrial (-40℃ to +85℃)
- **Cycling Endurance/Data Retention**
  - Typical 100k Program-Erase cycles on any sector
  - Typical 20-year data retention
- **Packages – JEDEC-standard, all RoHS-compliant**
  - TFBGA-24b05/6mm x 8mm (also known as TFBGA24)

Contents

1. Description

BY25QM1G1FS is a high-performance multiple input/output serial Flash memory device manufactured on 50nm NOR technology. It features execute-in-place (XIP) functionality, advanced write protection mechanisms, and a high-speed SPI-compatible bus interface. Innovative, high-performance, dual and quad input/output instructions enable double or quadruple the transfer bandwidth for Read and Program operations.

The 1Gb BY25QM1G1FS is a stacked device that contains four 256Mb die. From a user standpoint this stacked device behaves as a monolithic device, except with regard to Read Memory and Erase operations and status polling. The device contains a single chip select (/CS).

The memory is organized as 2048 (64KB) main sectors that are further divided into 16 subsectors each (32,768 subsectors in total). The memory can be erased one 4KB subsector at a time, 64KB sectors at a time, or single die (256Mb) at a time.

The memory can be write protected by software through volatile and nonvolatile protection features, depending on the application needs. The protection granularity is of 64KB (sector granularity) for volatile protections.

The device has 64 one-time Programmable (OTP) bytes that can be Read and Programmed with the Read OTP and Program OTP instructions. These 64 bytes can also be permanently locked with a Program OTP instruction.

The device also has the ability to pause and resume Program and Erase cycles by using dedicated Program /Erase Suspend and Resume instructions.

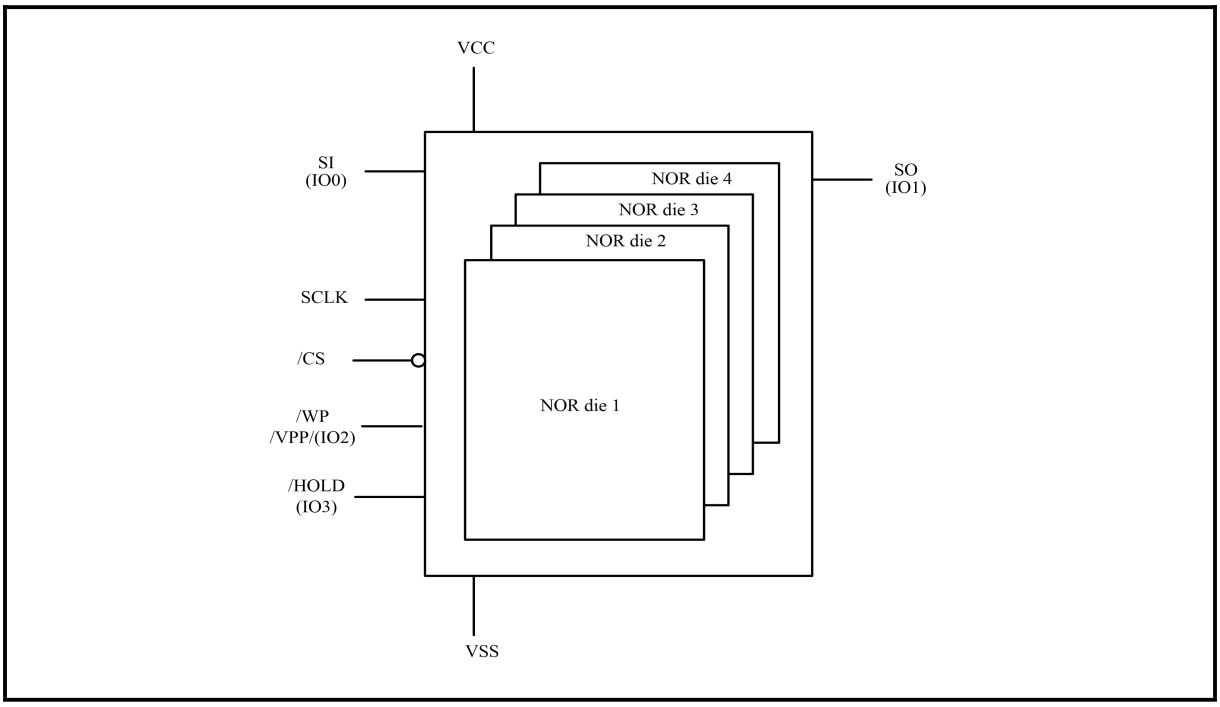
The memory can be operated with five different protocols:

- Extended SPI (standard SPI protocol upgraded with dual and quad operations)
- Dual I/O SPI
- Quad I/O SPI

The standard SPI protocol is extended and enhanced by dual and quad operations. In addition, the dual SPI and quad I/O SPI protocols improve the data access time and throughput of a single I/O device by transmitting instructions, addresses, and data across two or four data lines.

Each protocol contains unique instructions to perform Read operations in DTR mode. This enables high data throughput while running at lower clock frequencies.

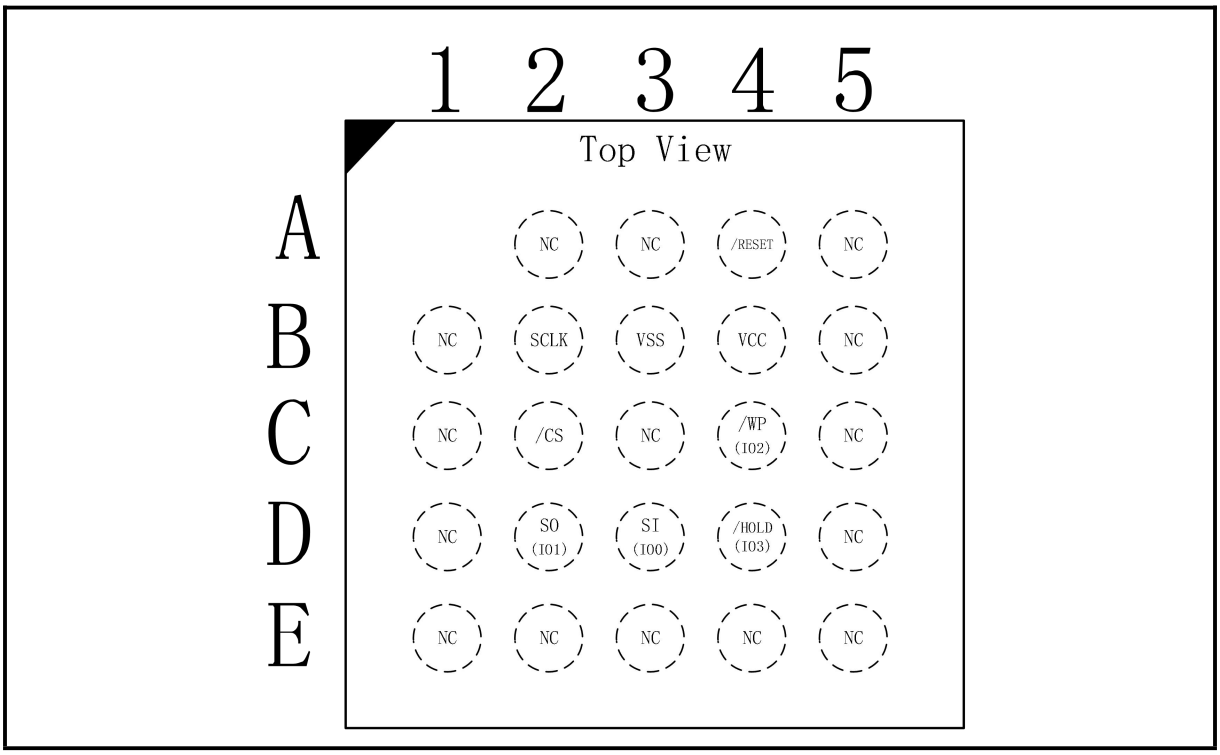
Figure 1. Logic diagram



Note:

1. Reset functionality is available in devices with a dedicated part number. See ***Part Number Information*** for more details.

Figure 2. Pin Configuration 24-Ball TFBGA 8X6mm (5x5 ball array)



2. Signal Description

2.1 Device Configurability

The BY25QM1G1FS offer additional features that are configured through the nonvolatile configuration register for default and/or nonvolatile settings. Volatile settings can be configured through the volatile and volatile-enhanced configuration registers. These configurable features include the following:

- Number of dummy cycles for the fast Read instructions
- Output buffer impedance
- SPI protocol types (extended SPI, DIO-SPI, or QIO-SPI)
- Required XIP mode
- Enabling/disabling HOLD (Reset function)
- Enabling/disabling wrap mode

2.2 Input/Output Summary

Table 1. Signal Descriptions

Pin Name	Type	Description
SCLK	Input	**Serial Clock**: This input signal provides the synchronization reference for the SPI interface. Instructions, addresses, or data input are latched on the rising edge of the SCLK signal. Data output changes after the falling edge of SCLK.
/CS	Input	**Chip Select:** When /CS is High, the device is deselected and SO is at High-Z. When in extended SPI mode, with the device deselected, SO is tri-stated. Unless an internal Program, Erase, or Write Status Register cycle is in progress, the device enters standby power mode (not deep power-down mode). Driving /CS Low enables the device, placing it in the active power mode. After power-up, a falling edge on /CS is required prior to the start of any instruction.
SI	Input and I/O	**Serial Data:** Transfers data serially into the device. It receives instruction codes, addresses, and the data to be Programmed. Values are latched on the rising edge of the clock. IQ0 is used for input/output during the following operations: Dual Output Fast Read, Quad Output Fast Read, Dual Input/Output Fast Read, and Quad Input/Output Fast Read. When used for output, data is shifted out on the falling edge of the clock. In DIO-SPI, IQ0 always acts as an input/output. In QIO-SPI, IQ0 always acts as an input/output, with the exception of the PROGRAM or ERASE cycle performed with VPP. The device temporarily enters the extended SPI protocol and then returns to QIO-SPI as soon as VPP goes low.
SO	output and I/O	**Serial data:** Transfers data serially out of the device. Data is shifted out on the falling edge of the clock. SO is used for input/output during the following operations: Dual Input Fast Program, Quad Input Fast Program, Dual Input Extended Fast Program, and Quad Input Extended Fast Program. When used for input, data is latched on the rising edge of the clock. In DIO-SPI, SO always acts as an input/output. In QIO-SPI, SO always acts as an input/output, with the exception of the Program or Erase cycle performed with the enhanced Program supply voltage (VPP). In this case the device temporarily enters the extended SPI protocol and then returns to QIO-SPI as soon as VPP goes LOW.
IO2	Input and I/O	**IO2:** When in QIO-SPI mode or in extended SPI mode using Quad Fast Read instructions, the signal functions as , providing input/output. All data input drivers are always enabled except when used as an output. BY Technology recommends customers drive the data signals normally (to avoid unnecessary switching current) and float the signals before the memory device drives data on them.
IO3	Input and I/O	**IO3:** When in quad SPI mode or in extended SPI mode using quad Fast Read instructions, the signal functions as , providing input/output. /HOLD is disabled and /RESET is disabled if the device is selected.
/HOLD	Control Input	**HOLD:** Pauses any serial communications with the device without deselecting the device. SO (output) is High-Z. SI (input) and the clock are "Don't Care." To enable HOLD, the device must be selected with /CS driven low. /HOLD is used for input/output during the following operations: Quad Output Fast Read, Quad Input/Output Fast Read, Quad Input Fast Program, and Quad Input Extended Fast Program. In QIO-SPI, /HOLD acts as an I/O (IO3 functionality), and the /HOLD functionality is disabled when the device is selected. When the device is deselected (/CS is HIGH) in parts with /RESET functionality, it is possible

Pin Name	Type	Description
		to reset the device unless this functionality is not disabled by means of dedicated registers bits. The /HOLD functionality can be disabled using bit 4 of the NVCR or bit 4 of the VECR. On devices that include DTR mode capability, the /HOLD functionality is disabled as soon as a DTR operation is recognized.
/WP	Control Input	**Write protect:** /WP can be used as a protection control input or in QIO-SPI operations. When in extended SPI with single or dual instructions, the Write Program function is selectable by the voltage range applied to the signal. If voltage range is low (0V to VCC), the signal acts as a write protection control input. The memory size protected against Program or Eease operations is locked as specified in the status register block protect bits 3:0. /WP is used as an input/output (functionality) during Quad Input Fast Read and Quad Input/Output Fast Read operations and in QIO-SPI.
VPP	Power	**Supply voltage:** If VPP is in the voltage range of VPPH, the signal acts as an additional power supply, as defined in the AC Measurement Conditions table. During QIFP, QIEFP, and QIO-SPI Program/Erase operations, it is possible to use the additional VPP power supply to speed up internal operations. However, to enable this functionality, it is necessary to set bit 3 of the VECR to 0. In this case, VPP is used as an I/O until the end of the operation. After the last input data is shifted in, the application should apply VPP voltage to VPP within 200ms to speed up the internal operations. If the VPP voltage is not applied within 200ms, the Program/Erase operations start at standard speed. The default value of VECR bit 3 is 1, and the VPP functionality for quad I/O modify operations is disabled.
VCC	Power	**Device core power supply:** Source voltage.
VSS	Ground	**Ground:** Reference for the VCC supply voltage
DNU	-	Do not use.
NC	-	No connect

3. Sector/Subsector Addresses

The memory is a stacked device comprised of four 256Mb chips. Each chip is internally partitioned into two 128Mb segments. Each page of memory can be individually programmed. Bits are from programmed one through zero. The device is subsector, sector, or single 256Mb chip erasable, but not page-erasable. Bits are erased from zero through one. The memory is configured as 134,217,728 bytes (8 bits each); 2048 sectors (64KB each); 32,768 subsectors (4KB each); and 524,288 pages (256 bytes each); and 64 OTP bytes are located outside the main memory array.

Figure 3. Block Diagram

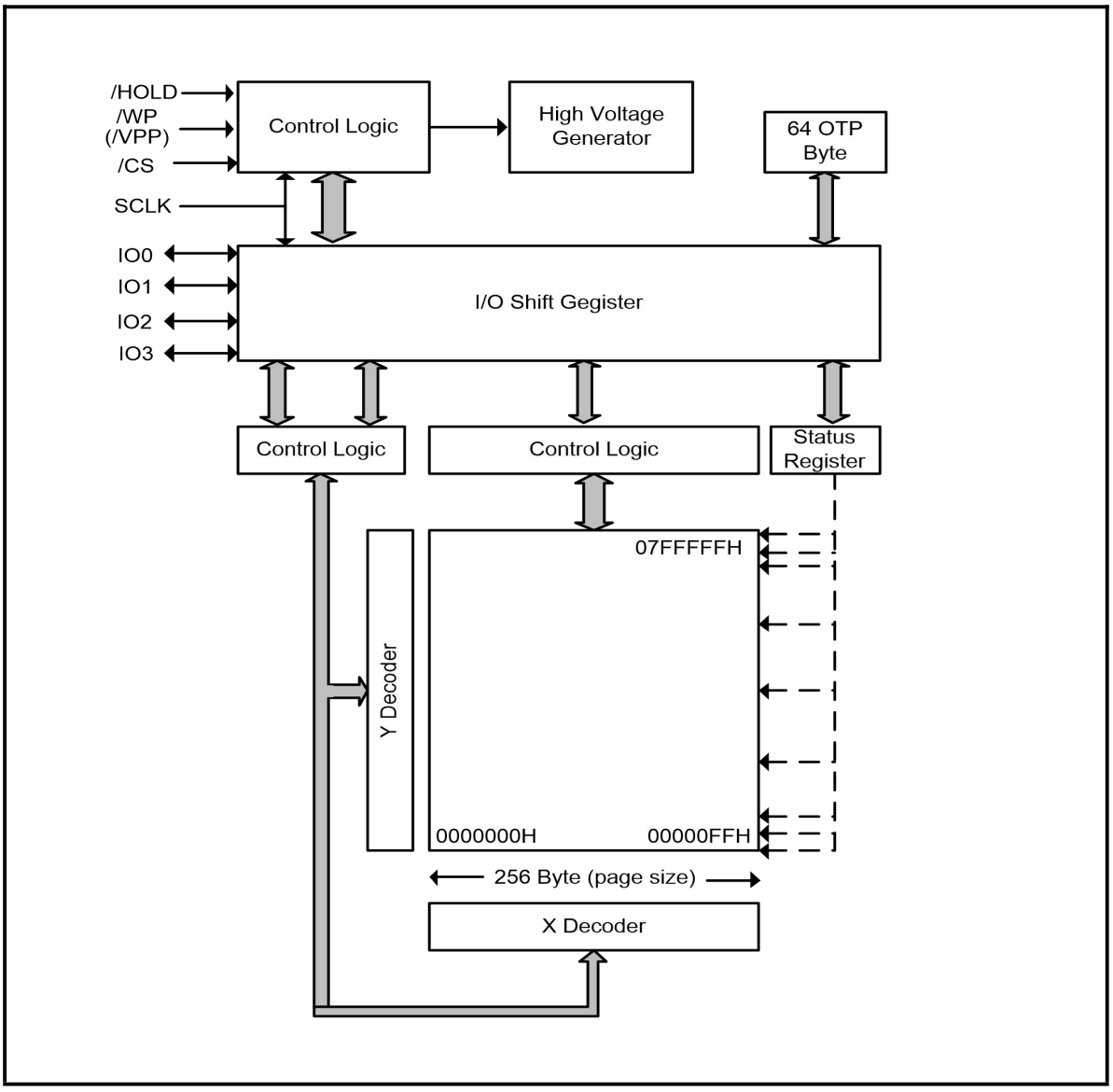


Table 2. The Chip Sector /Subsector Addresses of BY25QM1G1FS

Memory Density	Sector (64k byte)	Subsector No.	Subsector Size (KB)	Address range
1Gbit	Sector 0	Subsector 0	4	0000 0000h-0000 0FFFh
		⋮	⋮	⋮
		Subsector 15	4	0000 F000h-0000 FFFFh
	⋮	⋮	⋮	⋮
	Sector 63	Subsector 1008	4	003F 0000h-003F 0FFFh
		⋮	⋮	⋮
		Subsector 1023	4	003F F000h-003F FFFFh
	⋮	⋮	⋮	⋮
	Sector 127	Subsector 2032	4	007F 0000h-007F 0FFFh
		⋮	⋮	⋮
		Subsector 2047	4	007F F000h-007F FFFFh
	⋮	⋮	⋮	⋮
	Sector 255	Subsector 4080	4	00FF 0000h-00FF 0FFFh
		⋮	⋮	⋮
		Subsector 4095	4	00FF F000h-00FF FFFFh
	⋮	⋮	⋮	⋮
	Sector 511	Subsector 8176	4	01FF 0000h-01FF 0FFFh
		⋮	⋮	⋮
		Subsector 8191	4	01FF F000h-01FF FFFFh
	⋮	⋮	⋮	⋮
	Sector 1023	Subsector 16368	4	03FF 0000h-03FF 0FFFh
		⋮	⋮	⋮
		Subsector 16383	4	03FF F000h-03FF FFFFh
	⋮	⋮	⋮	⋮
	Sector 2047	Subsector 32750	4	07FF 0000h-07FF 0FFFh
		⋮	⋮	⋮
		Subsector 32767	4	07FF F000h-07FF FFFFh

Note:
1. Subsector = Uniform subsector, and the size is 4K bytes.
2. Sector = Uniform Sector, and the size is 64K bytes.
3. Big Block = 8 Sectors, e.g. Big Block 0 = Sector 0 - 7, and so on.

4. SPI Operation

4.1 Serial Peripheral Interface Modes

The device can be driven by a microcontroller while its serial peripheral interface is in either of the two modes shown here. The difference between the two modes is the clock polarity when the bus master is in standby mode and not transferring data. Input data is latched in on the rising edge of the clock, and output data is available from the falling edge of the clock.

Table 3. Protected Area Sizes – Lower Area

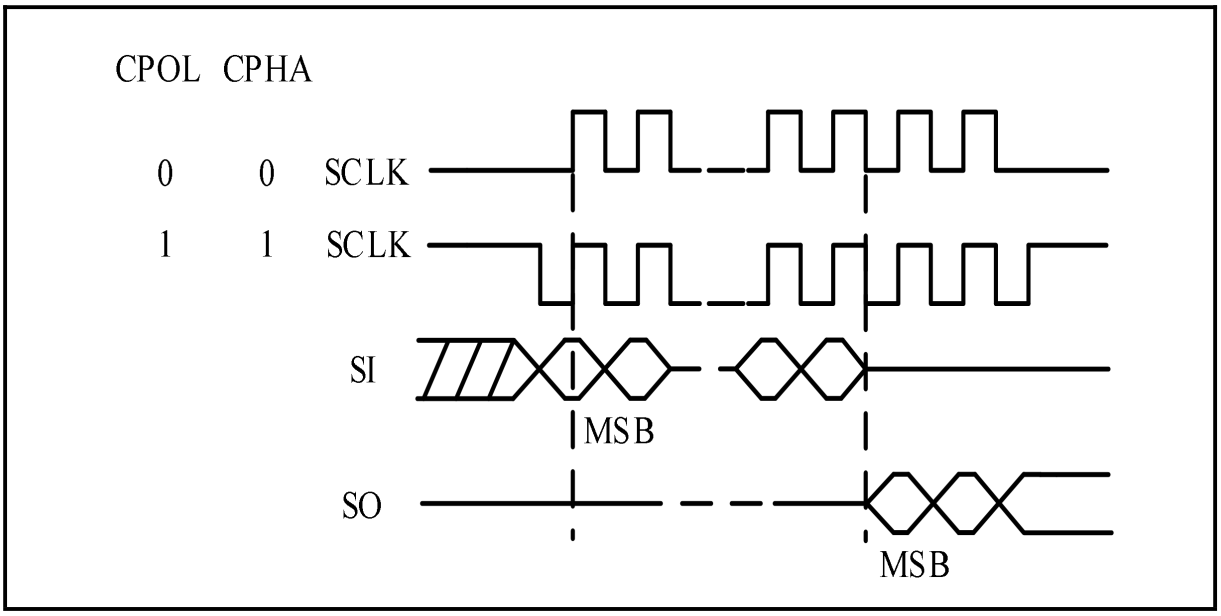
Note 1 applies to the entire table

SPI Modes	Clock polarity
CPOL = 0,CPHA = 0	C remains at 0 for (CPOL = 0, CPHA = 0)
CPOL = 1,CPHA = 1	C remains at 1 for (CPOL = 1, CPHA = 1)

Note：

1. The listed SPI modes are supported in extended, dual, and quad SPI protocols.

Figure 4. SPI Modes



4.2 SPI Protocol

Table 4. Extended, Dual, and Quad SPI Protocols

Protocol Name	Comm-and input	Address Input	Data Input/ Output	Description
Extended	SI	Multiple IOn lines,de-pending on the instruction	Multiple IOn lines,de-pending on the instruction	Device default protocol from the factory. Additional instructions extend the standard SPI protocol and enable address or data transmission on multiple IOn lines.
Dual	IO[1:0]	IO[1:0]	IO[1:0]	**Volatile selectable:** When the enhanced volatile configuration register bit 6 is set to 0 and bit 7 is set to 1, the device enters the dual SPI protocol immediately after the Write Enhanced Volatile Configuration Register instruction. The device returns to the default protocol after the next power-on. In addition, the device can return to default protocol using the rescue sequence or through new Write Enhanced Volatile Configuration Register instruction, without power-off or power-on. **Nonvolatile selectable:** When nonvolatile configuration register bit 2 is set, the device enters the dual SPI protocol after the next power-on. Once this register bit is set, the device defaults to the dual SPI protocol after all subsequent power-on sequences until the nonvolatile configuration register bit is reset to 1.
Quad[1]	IO[3:0]	IO[3:0]	IO[3:0]	**Volatile selectable:** When the enhanced volatile configuration register bit 7 is set to 0, the device enters the quad SPI protocol immediately after the Write Enhanced Volatile Configuration Register instruction. The device returns to the default protocol after the next power-on. In addition, the device can return to default protocol using the rescue sequence or through new Write Enhanced Volatile Configuration Register instruction, without power-off or power-on. **Nonvolatile selectable:** When nonvolatile configuration register bit 3 is set to 0, the device enters the quad SPI protocol after the next power-on. Once this register bit is set, the device defaults to the quad SPI protocol after all subsequent power-on sequences until the nonvolatile configuration register bit is reset to 1.

Note:

1. In quad SPI protocol, all instruction/address input and data I/O are transmitted on four lines except during a Program and Erase cycle performed with VPP. In this case, the device enters the extended SPI protocol to temporarily allow the application to perform a Program / Erase Suspend operation or to check the write-in-progress bit in the status register or the Program/erase controller bit in the flag status register. Then, when VPP goes Low, the device returns to the quad SPI protocol.

5. Operation Features

5.1 Supply Voltage

5.1.1 Operating Supply Voltage

Prior to selecting the memory and issuing instructions to it, a valid and stable VCC voltage within the specified [VCC(min), VCC(max)] range must be applied (see ***Electrical Characteristics***). In order to secure a stable DC supply voltage, it is recommended to decouple the VCC line with a suitable capacitor (typically 100nF) close to the VCC/VSS package pins. This voltage must remain stable and valid until the end of the transmission of the instruction and, for a Write instruction, until the completion of the internal write cycle (tW).

5.1.2 Power-up Conditions

When the power supply is turned on, VCC rises continuously from VSS to VCC. During this time, the Chip Select (/CS) line is not allowed to float but should follow the VCC voltage, it is therefore recommended to connect the /CS line to VCC via a suitable pull-up resistor.

In addition, the Chip Select (/CS) input offers a built-in safety feature, as the /CS input is edge sensitive as well as level sensitive: after power-up, the device does not become selected until a falling edge has first been detected on Chip Select (/CS). This ensures that Chip Select (/CS) must have been high, prior to going low to start the first operation. During a standard power-up phase, the device ignores all instructions except Read Status Register and Read Flag Status Register. These operations can be used to check the memory internal state.

5.1.3 Device Reset

In order to prevent data corruption inadvertent Write operations during power-up (continuous rise of VCC), a power on reset (POR) circuit is included. At Power-up, the device does not respond to an instruction until VCC has reached the power on reset threshold voltage (this threshold is lower than the minimum VCC operating voltage defined in ***Power-up Timing***).

5.1.4 Power-down

At Power-down (continuous decrease in VCC), as soon as VCC drops from the normal operating voltage to below the power on reset threshold voltage, the device stops responding to any instruction sent to it. During Power-down, the device must be deselected (Chip Select (/CS) should be allowed to follow the voltage applied on VCC) and in Standby Power mode (that is there should be no internal Write cycle in progress).

5.2 Active Power and Standby Power Modes

When Chip Select (/CS) is Low, the device is selected, and in the Active Power mode. The device consumes ICC.

When Chip Select (/CS) is High, the device is deselected. If a Write cycle is not currently in progress, the device then goes in to the Standby Power mode, and the device consumption drops to ICC1.

5.3 Power Loss Recovery Sequence

If a power loss occurs during a WRITE NONVOLATILE CONFIGURATION REGISTER instruction, after the next power-on, the device might begin in an undetermined state (XIP mode or an unnecessary protocol). If this occurs, until the next power-up, a recovery sequence must reset the device to a fixed state (extended SPI protocol without XIP). After the recovery sequence, the issue should be resolved definitively by running the WRITE NONVOLATILE CONFIGURATION REGISTER instruction again. The recovery sequence is composed of two parts that must be run in the correct order. During the entire sequence, tSHSL2 must be at least 50ns. The first part of the sequence is IO0 (SI) and IO3 (HOLD) equal to 1 for the situations listed below:

- 7 clock cycles within /CS LOW (/CS becomes HIGH before 8th clock cycle)
- + 9 clock cycles within /CS LOW (/CS becomes HIGH before 10th clock cycle)
- + 13 clock cycles within /CS LOW (/CS becomes HIGH before 14th clock cycle)
- + 17 clock cycles within /CS LOW (/CS becomes HIGH before 18th clock cycle)
- + 25 clock cycles within /CS LOW (/CS becomes HIGH before 26th clock cycle)
- + 33 clock cycles within /CS LOW (/CS becomes HIGH before 34th clock cycle)

The second part of the sequence is exiting from dual or quad SPI protocol by using the following FFh sequence: IO0 and IO3 equal to 1 for 8 clock cycles within /CS LOW; /CS becomes HIGH before 9th clock cycle.

After this two-part sequence the extended SPI protocol is active.

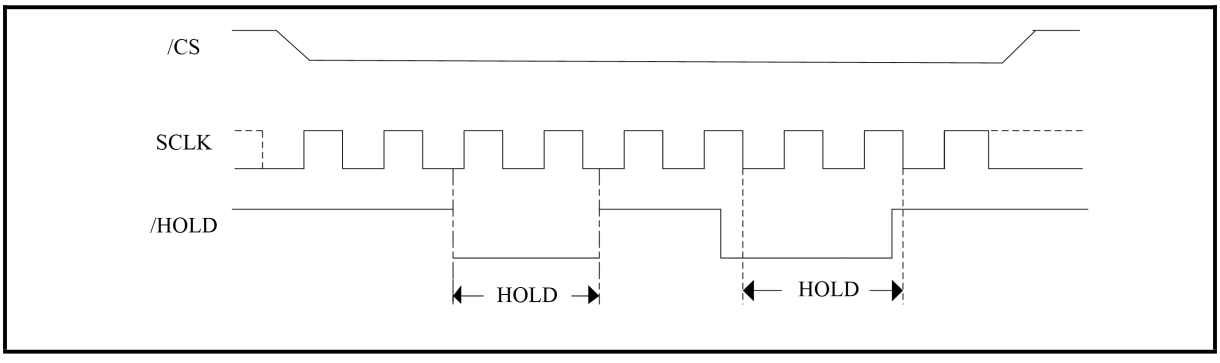
5.4 Hold Condition

The Hold (/HOLD) signal is used to pause any serial communications with the device without resetting the clocking sequence. During the Hold condition, the SO is high impedance, and SI and Serial Clock (SCLK) are Don't Care. To enter the Hold condition, the device must be selected, with Chip Select (/CS) low. Normally, the device is kept selected, for the whole duration of the Hold condition. Deselecting the device while it is in the Hold condition, has the effect of resetting the state of the device, and this mechanism can be used if it is required to reset any processes that had been in progress.

On devices that include the DTR mode function, once the DTR operation is recognized, the /HOLD function will be disabled.

The Hold condition starts when the Hold (/HOLD) signal is driven Low at the same time as Serial Clock (SCLK) already being Low (as shown in ***Figure 5)***. The Hold condition ends when the Hold (HOLD) signal is driven high at the same time as Serial Clock (SCLK) already being Low. ***Figure 5*** also shows what happens if the rising and falling edges are not timed to coincide with Serial Clock (SCLK) being low.

Figure 5. Hold condition activation



5.5 Protection Features

1. Software Protection (Memory array):

   - The Block Protect (BP4, BP3, BP2, BP1, BP0) bits define the section of the memory array that can be read but not change (see the ***Table 6*** and ***Table 7***)

   - The device can configure the sector lock register through Write Lock Register Instruction to lock the specified sector. Sector Lock Register bits 1:0 are written to by the Write Lock Register instruction. The instruction will not execute unless the sector lock down bit is cleared (see the Memory Sector Protection Truth Table). After power-up, the devices is in standby power mode; the write enable latch bit is reset; the write in progress bit is reset; and the lock registers are configured as: (write lock bit, lock down bit) = (0,0).

2. Hardware Protection (Status register): /WP can be used as a protection control input. When in extended SPI with single or dual instructions, the Write Protect function is selectable by the voltage range applied to the signal. If voltage range is low (0V), the signal acts as a write protection control input. Used with the /WP signal to enable or disable writing to the status register. When the enable/disable bit is set to 1, and the /W/VPP signal is driven Low, the status register nonvolatile bits become Read-only and the Write Status Register operation will not execute. The only way to exit this hardware-protected mode is to drive /WP/VPP High.

3. Device resets when VCC is below threshold: Upon power-up or at power-down, the BY25QM1G1FS will maintain a reset condition while VCC is below the threshold value of VWI. While reset, all operations are disabled and no instructions are recognized.

4. Time delay write disable after Power-up: During power-up and after the VCC voltage exceeds VCC (min), all Program and erase related instructions are further disabled for a time delay of tVSL. This includes the Write Enable, Page Program, Subsector Erase, Sector Erase, Die Erase and the Write Status Register instructions.

5. Write Enable: The Write Enable instruction is set the Write Enable Latch bit. Ensures that instructions modifying device data must be preceded by a Write Enable instruction, which sets the write enable latch bit in the status register. The Write Enable Latch bit will return to reset by following situation:

   -Power –up
   -Write Disable
   -Write Status Register (Whether the SR is protected, WEL will return to reset)
   -Program Operations/ (Whether the program area is protected, WEL will return to reset)
   -Program OTP Array (When the operation is times out)
   -Subsector Erase/Sector Erase/Die Erase (Whether the erase area is protected, WEL will return to reset)
   -Clear Flag Status Register (In case of a protection error)
   -Software Reset
   -Hardware Reset

6. Power-on reset and internal timer: Protects the device against inadvertent data changes while the power supply is outside the operating specification.

Table 5. Memory Sector Protection Truth Table

Note 1 applies to the entire table

Sector Lock Register		Memory Sector Protection Status
Sector Lock Down Bit	Sector Write Lock Bit	
0	0	Sector unprotected from Program and Erase operations. Protection status reversible
0	1	Sector protected from Program and Erase operations. Protection status reversible
1	0	Sector unprotected from Program and Erase operations. Protection status not reversible except by power cycle or reset.
1	1	Sector protected from Program and Erase operations. Protection status not reversible except by power cycle or reset.

Note：

1. Sector lock register bits are written to when the Write to Lock Register instruction is executed. The instruction will not execute unless the sector lock down bit is cleared (see the Lock Register).

Table 6.Protected Area Sizes – Upper Area

Note 1 applies to the entire table

Status Register Content					Memory Content	
BP4	BP3	BP2	BP1	BP0	Protected Area	Unprotected Area
0	0	0	0	0	None	All sectors
0	0	0	0	1	Sector 2047	Sectors (0 to 2046)
0	0	0	1	0	Sectors (2046 to 2047)	Sectors (0 to 2045)
0	0	0	1	1	Sectors (2044 to 2047)	Sectors (0 to 2043)
0	0	1	0	0	Sectors (2040 to 2047)	Sectors (0 to 2039)
0	0	1	0	1	Sectors (2032 to 2047)	Sectors (0 to 2031)
0	0	1	1	0	Sectors (2016 to 2047)	Sectors (0 to 2015)
0	0	1	1	1	Sectors (1984 to 2047)	Sectors (0 to 1983)
0	1	0	0	0	Sectors (1920 to 2047)	Sectors (0 to 1919)
0	1	0	0	1	Sectors (1792 to 2047)	Sectors (0 to 1791)
0	1	0	1	0	Sectors (1536 to 2047)	Sectors (0 to 1535)
0	1	0	1	1	Sectors (1024 to 2047)	Sectors (0 to 1023)
0	1	1	0	0	All sectors	None
0	1	1	0	1	All sectors	None
0	1	1	1	0	All sectors	None
0	1	1	1	1	All sectors	None

Note：

1. See the Status Register for details on the BP 4 bit and the BP 3:0 bits.

Table 7.Protected Area Sizes – Lower Area

Note 1 applies to the entire table

Status Register Content					Memory Content	
BP4	BP3	BP2	BP1	BP0	Protected Area	Unprotected Area
1	0	0	0	0	None	All sectors
1	0	0	0	1	Sector 0	Sectors (1 to 2047)
1	0	0	1	0	Sectors (0 to 1)	Sectors (2 to 2047)
1	0	0	1	1	Sectors (0 to 3)	Sectors (4 to 2047)
1	0	1	0	0	Sectors (0 to 7)	Sectors (8 to 2047)
1	0	1	0	1	Sectors (0 to 15)	Sectors (16 to 2047)
1	0	1	1	0	Sectors (0 to 31)	Sectors (32 to 2047)
1	0	1	1	1	Sectors (0 to 63)	Sectors (64 to 2047)
1	1	0	0	0	Sectors (0 to 127)	Sectors (128 to 2047)
1	1	0	0	1	Sectors (0 to 255)	Sectors (256 to 2047)
1	1	0	1	0	Sectors (0 to 511)	Sectors (512 to 2047)
1	1	0	1	1	Sectors (0 to 1023)	Sectors (1024 to 2047)
1	1	1	0	0	All sectors	None
1	1	1	0	1	All sectors	None
1	1	1	1	0	All sectors	None
1	1	1	1	1	All sectors	None

Note：

1. See the Status Register for details on the BP 4 bit and the BP 3:0 bits.

5.6 Nonvolatile and Volatile Registers

The device features the following volatile and nonvolatile registers that users can access to store device parameters and operating configurations:

- Status register
- Nonvolatile and volatile configuration registers
- Extended address register
- Enhanced volatile configuration register
- Flag status register
- Lock register

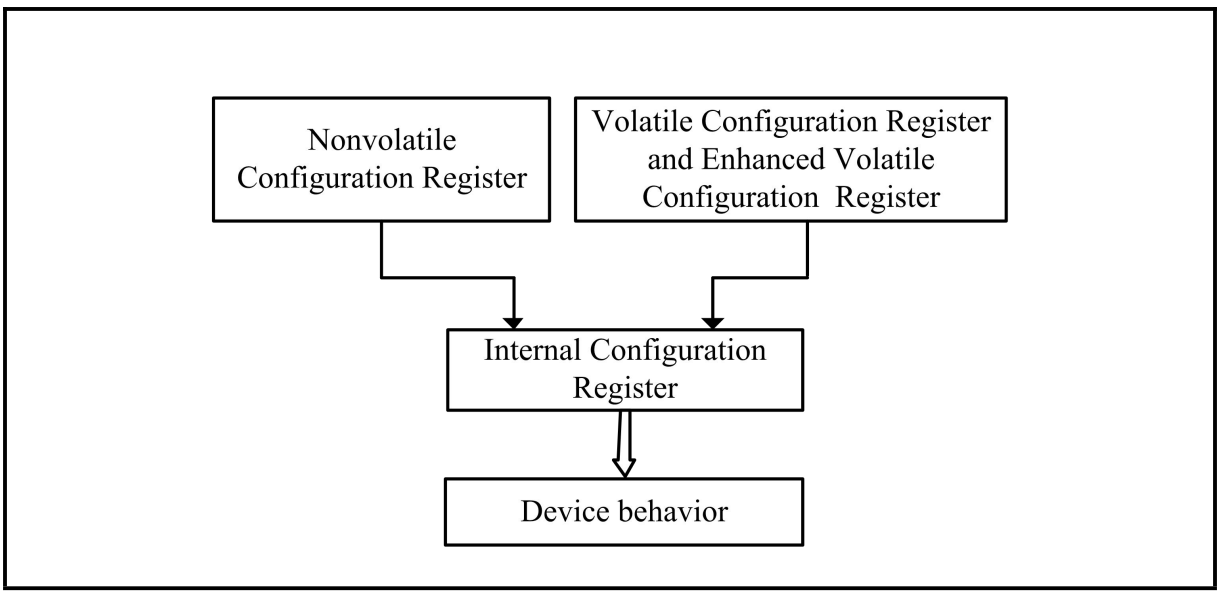
The working condition of memory is set by an internal configuration register that is not directly accessible to users (see the ***Figure 6***). As shown below, parameters in the internal configuration register are loaded from the nonvolatile configuration register during each device boot phase or power-on reset. In this sense, then, the nonvolatile configuration register contains the default settings of memory.

Also, during the life of an application, each time a Write Volatile or Enhanced Volatile Configuration Register instruction executes to set configuration parameters in these respective registers, these new settings are copied to the internal configuration register. Therefore, memory settings can be changed in real time. However, at the next power-on reset, the memory boots according to the memory settings defined in the nonvolatile configuration register parameters.

The device behavior of the memory is ultimately determined by the Internal Configuration Register. The Internal Configuration Register can choose to download instruction data from Nonvolatile configuration register or Volatile configuration register and enhanced volatile configuration register according to different situations.

Nonvolatile configuration register download is executed only during the power-on phase or after a reset, overwriting configuration register. Volatile configuration register and enhanced volatile configuration register download is executed after a write Volatile or Enhanced volatile configuration register instruction, overwrite configuration register setting on internal configuration register.

Figure 6. Internal Configuration Register



5.5.1 Status Register

Table 8. Status Register Bit Definitions

Bit	Name	Settings	Description	Note
7	Status Register Write Enable/Disable	0 = Enabled 1 = disabled	**Nonvolatile bit:** Used with the /WP signal to enable or disable writing to the status register.	3
5	Block Protect 4	0 = Top 1 = Bottom	**Nonvolatile bit:** Determines whether the protected memory area defined by the block protect bits starts from the top or bottom of the memory array.	4
6,4:2	Block Protect 3-0	See Protected Area Sizes – Upper Area and Lower Area tables in Device Protection	**Nonvolatile bit:** Defines memory to be software protected against Program or Erase operations. When one or more block protect bits is set to 1, a designated memory area is protected from Program and Erase operations.	4
1	Write Enable Latch	0 = Cleared 1 = Set	**Volatile bit:** The device always powers up with this bit cleared to prevent inadvertent Write Status Register, Program, or Erase operations. To enable these operations, the Write Enable operation must be executed first to set this bit.	2,5
0	Write in Progress	0 = Ready (Default) 1 = Busy	**Volatile bit:** Indicates if one of the following instruction cycles is in progress: Write Status Register, Write Nonvolatile Configuration Register, Program, Erase.	2,6

Note:

1. Bits can be Read from or written to using Read Status Register or Write Status Register instructions, respectively.
2. Volatile bits are cleared to 0 by a power cycle or reset.
3. The status register write enable/disable bit, combined with the /WP/VPP signal as described in the Signal Descriptions, provides hardware data protection for the device as follows: When the enable/disable bit is set to 1, and the /WP/VPP signal is driven low, the status register nonvolatile bits become Read-only and the Write Status Register operation will not execute. The only way to exit this hardware-protected mode is to drive /WP/VPP high.
4. See Protected Area Sizes ***Table 6*** and ***Table 7.*** The Die Erase instruction is executed only if all bits are 0.
5. In case of protection error this volatile bit is set and can be reset only by means of a Clear Flag Status Register instruction.
6. Program or erase controller bit = NOT (write in progress bit).

5.6.2 Nonvolatile and Volatile Configuration Registers

Table 9. Nonvolatile Configuration Register Bit Definitions

Note 1 applies to the entire table

Bit	Name	Settings	Description	Note
15:12	Number of Dummy clock cycles	0000 (identical to 1111，default) 0001 0010 . . 1101 1110 1111	Sets the number of dummy clock cycles subsequent to all Fast Read instructions. The default setting targets the maximum allowed frequency and guarantees backward compatibility.	2,3
11:9	XIP Mode at Power-on Reset	000 = XIP: Fast Read 001 = XIP: Dual Output Fast Read 010 = XIP: Dual I/O Fast Read 011 = XIP: Quad Output Fast Read 100 = XIP: Quad I/O Fast Read 101 = Reserved 110 = Reserved 111 = Disabled (Default)	Enables the device to operate in the selected XIP mode immediately after power-on reset.	
8:6	Output Driver Strength	000 = Reserved 001 = 90 Ohms 010 = 60 Ohms 011 = 45 Ohms 100 = Reserved 101 = 20 Ohms 110 = 15 Ohms 111 = 30 (Default)	Optimizes impedance at VCC/2 output voltage.	
5	Reserved	X	"Don't Care."	
4	Reset/hold	0 = Disabled 1 = Enabled (Default)	Enables or disables hold or reset. (Available on dedicated part numbers.)	
3	Quad I/O Protocol	1 = Disabled (Default, Extended SPI protocol)	Enables or disables quad I/O protocol.	4
2	Dual I/O Protocol	0 = Enabled 1 = Disabled (Default, Extended SPI protocol)	Enables or disables dual I/O protocol.	4
1	128Mb Segment Select	0 = Upper 128Mb segment 1 = Lower 128Mb segment (Default)	Selects a 128Mb segment as default for 3Byte address operations. See also the extended address register.	
0	Address Bytes	0 = Enable 4B address 1 = Enable 3B address (Default)	Defines the number of address bytes for a instruction.	

Note:

1. Settings determine device memory configuration after power-on. The device ships from the factory with all bits erased to 1 (FFFFh). The register is Read from or written to by Read Nonvolatile Configuration Register or Write Nonvolatile Configuration instructions, respectively.
2. The 0000 and 1111 settings are identical in that they both define the default state, which is the maximum frequency of fc = 108MHz. This ensures backward compatibility.
3. If the number of dummy clock cycles is insufficient for the operating frequency, the memory reads wrong data. The number of cycles must be set according to and sufficient

for the clock frequency, which varies by the type of Fast Read instruction, as shown in the Supported Clock Frequencies table.

4. If bits 2 and 3 are both set to 0, the device operates in quad I/O. When bits 2 or 3 are reset to 0, the device operates in dual I/O or quad I/O respectively, after the next power-on.

Table 10. Volatile Configuration Register Bit Definitions

Note 1 applies to the entire table

Bit	Name	Settings	Description	Note
7:4	Number of Dummy Clock Cycles	0000 (identical to 1111, default) 0001 0010 . . 1101 1110 1111	Sets the number of dummy clock cycles subsequent to all Fast Read instructions. The default setting targets maximum allowed frequency and guarantees backward compatibility.	2,3
3	XIP	0 1	Enables (XIP bit=0) or disables XIP (XIP bit=1). For device part numbers with feature digit equal to 2 or 4, this bit is always "Don't Care," so the device operates in XIP mode without setting this bit.	
2	Reserved	x = Default	1b = Fixed value.	
1:0	Wrap	00 = 16-byte boundary aligned	16-byte wrap: Output data wraps within an aligned 16-byte boundary starting from the address (3-byte or 4-byte) issued after the instruction code.	4
		01 = 32-byte boundary aligned	32-byte wrap: Output data wraps within an aligned 32-byte boundary starting from the address (3-byte or 4-byte) issued after the instruction code.	
		10 = 64-byte boundary aligned	64-byte wrap: Output data wraps within an aligned 64-byte boundary starting from the address (3-byte or 4-byte) issued after the instruction code.	
		11 = sequential (default)	Continuous Reading (default): All bytes are Read sequentially.	

Note:

1. Settings determine the device memory configuration upon a change of those settings by the Write Volatile Configuration Register instruction. The register is Read from or written to by Read Volatile Configuration Register or Write Volatile Configuration Register instructions respectively.
2. The 0000 and 1111 settings are identical in that they both define the default state which is the maximum frequency of fc = 108MHz. This ensures backward compatibility.
3. If the number of dummy clock cycles is insufficient for the operating frequency, the memory Read wrong data. The number of cycles must be set according to and be sufficient for the clock frequency, which varies by the type of Fast Read instruction, as shown in the Supported Clock Frequencies ***Table 12.***
4. See the Sequence of Bytes During Wrap table (as show in ***Table 11***).

Table 11. Sequence of Bytes During Wrap

Starting Address	16-Byte Wrap	32-Byte Wrap	64-Byte Wrap
0	0-1-2-…-15-0-1- …	0-1-2-…-31-0-1-…	0-1-2-…-63-0-1-…
1	1-2-…-15-0-1-2-…	1-2-…-31-0-1-2-…	1-2-…-63-0-1-2-…
15	15-0-1-2-3-…-15-0-1-…	15-16-17-…-31-0-1-…	15-16-17-…-63-0-1-…
31	31-16-17-…-31-16-17- …	31-0-1-2-3-…-31-0-1-…	31-32-33-…-63-0-1-…
63	63-48-49-…-63-48-49-…	63-32-33-…-63-32-33-…	63-0-1-…-63-0-1-…

Table 12. Supported Clock Frequencies – STR

Note 1 applies to entire table

Number of Dummy Clock Cycles	FAST READ	DUAL OUTPUT FAST READ	DUAL I/O FAST READ	QUAD OUTPUT FAST READ	QUAD I/O FAST READ
1	90	80	50	43	30
2	100	90	70	60	40
3	108	100	80	75	50
4	108	105	90	90	60
5	108	108	100	100	70
6	108	108	105	105	80
7	108	108	108	108	86
8	108	108	108	108	95
9	108	108	108	108	105
10	108	108	108	108	108

Note:
1. Values are guaranteed by characterization and not 100% tested in production.

Table 13. Supported Clock Frequencies – DTR

Note 1 applies to entire table

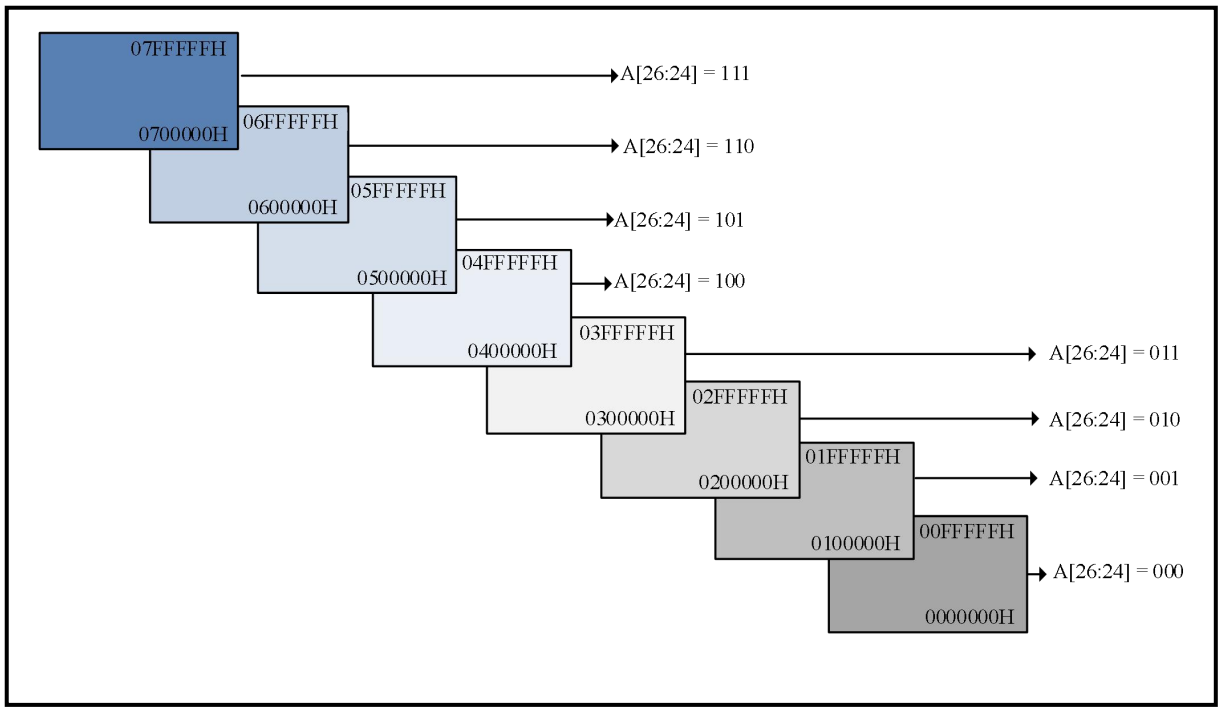
Number of Dummy Clock Cycles	FAST READ	DUAL OUTPUT FAST READ	DUAL I/O FAST READ	QUAD OUTPUT FAST READ	QUAD I/O FAST READ
1	45	40	25	30	15
2	50	45	35	38	20
3	54	50	40	45	25
4	54	53	45	47	30
5	54	54	50	50	35
6	54	54	54	53	40
7	54	54	54	54	43
8	54	54	54	54	48
9	54	54	54	54	53
10	54	54	54	54	54

Note:
1. Values are guaranteed by characterization and not 100% tested in production.

5.6.3 Extended Address Register

In the case of 3-byte addressability mode, the device includes an extended address register that provides a fourth address byte A[31:24], enabling access to memory beyond 128Mb. The extended address register bits [2:0] are used to select one of the eight 128Mb segments of the memory array.

Figure 7. Upper and Lower Memory Array Segments



The Program and Erase operations act upon the 128Mb segment selected in the extended address register.

The Read operation begins Reading in the selected 128Mb segment. It is bound by the 256Mb (die segment) to which the 128Mb segment belongs. In a continuous Read, when the last byte of the die segment selected is Read, the next byte output is the first byte of the same die segment; therefore, a download of the whole array is not possible with one Read operation. The value of the extended address register does not change when a Read operation crosses the selected 128Mb boundary.

Table 14. Extended Address Register Bit Definitions

Note 1 applies to entire table

Bit	Name	Settings	Description
7 6 5 4 3	A[31:27]	0 = Reserved	
2 1 0	A[26:24]	111 = Upper 128Mb segment 110 = Seventh 128Mb segment 101 = Sixth 128Mb segment 100 = Fifth 128Mb segment 011 = Fourth 128Mb segment 010 = Third 128Mb segment 001 = Second 128Mb segment 000 = Lower 128Mb segment (default)	Enable selecting 128Mb segmentation. For A[26:24], the default setting is determined by bit 1 of the nonvolatile configuration register. However, this setting can be changed using the Write Extended Address Register instruction.

Note:

1. The extended address register is for an application that supports only 3-byte addressing. It extends the device's first three address bytes A[23:0] to a fourth address byte A [31:24] to enable memory access beyond 128Mb. The extended address register bits [2:0] are used to select one of the eight 128Mb segments of the memory array. If 4-byte addressing is enabled, extended address register settings are ignored.

5.6.4 Enhanced Volatile Configuration Register

Table 15. Enhanced Volatile Configuration Register Bit Definitions

Note 1 applies to entire table

Bit	Name	Settings	Description	Note
7	Quad I/O Protocol	0 = Enabled 1 = Disabled (Default, extended SPI protocol)	Enables or disables quad I/O protocol.	2
6	Dual I/O Protocol	0 = Enabled 1 = Disabled (Default, extended SPI protocol)	Enables or disables dual I/O protocol.	2
5	Reserved	x = Default	1b = Fixed value.	
4	Reset/hold	0 = Disabled 1 = Enabled (Default)	Enables or disables hold or reset. (Available on dedicated part numbers.)	
3	VPP Accelerator	0 = Enabled 1 = Disabled (Default)	Enables or disables VPP acceleration for Quad Input Fast Program , Quad Input Extended Fast Program Operations in Extended and Quad SPI Protocols; Enables or disables VPP acceleration for Page Program, Dual Input Fast Program, Extended Dual Input Fast Program, Subsector Erase, Sector Erase, Die Erase Operations in Quad SPI Protocols.	
2:0	Output Driver Strength	000 = Reserved 001 = 90 Ohms 010 = 60 Ohms 011 = 45 Ohms 100 = Reserved 101 = 20 Ohms 110 = 15 Ohms 111 = 30 (Default)	Optimizes impedance at VCC/2 output voltage.	

Note:

1. Settings determine the device memory configuration upon a change of those settings by the Write Enhanced Volatile Configuration Register instruction. The register is Read from or written to in all protocols by Read Enhanced Volatile Configuration Register or Write Enhanced Volatile Configuration Register instructions, respectively.
2. If bits 6 and 7 are both set to 0, the device operates in quad I/O. When either bit 6 or 7 is reset to 0, the device operates in dual I/O or quad I/O respectively following the next Write Enhanced Volatile Configuration Register instruction.

5.6.5 Flag Status Register

Table 16. Flag Status Register Bit Definitions

Note 1 applies to entire table

Bit	Name	Settings	Description	Note
7	Program or Erase Controller	0 = Busy 1 = Ready (default)	Status bit: Indicates whether one of the following instruction cycles is in progress: Write Status Register, Write Nonvolatile Configuration Register, Program, or Erase.	2, 5
6	Erase suspend	0 = Not in effect (default) 1 = In effect	Status bit: Indicates whether an Erase operation has been or is going to be suspended.	2
5	Erase	0 = Clear (default) 1 = Failure or protection error	Error bit: Indicates whether an Erase operation has succeeded or failed.	3, 4
4	Program	0 = Clear (default) 1 = Failure or protection error	Error bit: Indicates whether a PROGRAM operation has succeeded or failed.	3, 4
3	VPP	0 = Enabled (Default) 1 = Disabled	Error bit: Indicates an invalid voltage on VPP during a Program or Erase operation.	3, 4
2	Program Suspend	0 = Not in effect (default) 1 = In effect	Status bit: Indicates whether a Program operation has been or is going to be suspended.	2
1	Protection	0 = Clear (default) 1 = Failure or protection error	Error bit: Indicates whether an Erase or Program operation has attempted to modify the protected array sector, or whether a Program operation has attempt ted to access the locked OTP space.	3,4
0	Addressing	0 = 3 bytes addressing (default) 1 = 4 bytes addressing	Status bit: Indicates whether 3-byte or 4-byte address mode is enabled.	2

Note:

1. Register bits are Read by Read Flag Status Register instruction. All bits are volatile.
2. Status bits are reset automatically.
3. Error bits must be cleared through the Clear Flag Status Register instruction.
4. These error flags are "sticky." They must be cleared through the Clear Status Register instruction.
5. Program or erase controller bit = NOT (write in progress bit).

5.6.6 Lock Register

Table 17. Lock Register Bit Definitions

Note 1 applies to entire table

Bit	Name	Settings	Description
7:2	Reserved	0	Bit values are 0.
1	Write Lock Down	0 = Cleared (Default) 1 = Set	**Volatile bit:** the device always powers-up with this bit cleared, which means sector lock down and sector write lock bits can be set. When this bit set, neither of the lock register bits can be written to until the next power cycle.
0	Sector Write Lock	0 = Cleared (Default) 1 = Set	**Volatile bit:** the device always powers-up with this bit cleared, which means that Program and Erase operations in this sector can be executed and sector content modified. When this bit is set, Program and Erase operations in this sector will not be executed.

Note:
1. Sector lock register bits 1:0 are written to by the Write Lock Register instruction. The instruction will not execute unless the sector lock down bit is cleared.

5.7 3-Byte/4-Byte Address Modes

The device features 3-byte or 4-byte address modes to access memory beyond 128Mb.

When 4-byte address mode is enabled, all instructions requiring an address must be Entered and Exited with a 4-byte address mode instruction: Enter 4-Byte Address Mode instruction and Exit 4-Byte Address Mode instruction. The 4-byte address mode can also be enabled through the non-volatile configuration register.

Reading and writing to an A[MAX:MIN] of A[31:0] (4-byte address) is also supported. Selection of the 3-byte or 4-byte address range can be enabled in two ways: through the nonvolatile configuration register or through the Enable 4-Byte Address Mode/Exit 4-Byte Address Mode instructions. Further details for these settings and instructions are in the respective register and instruction sections of the data sheet.

5.8 XIP Mode

XIP mode requires only an address (no instruction) to output data, improving random access time and eliminating the need to shadow code onto RAM for fast execution. All protocols support XIP operation. For flexibility, multiple XIP entry and exit methods are available. For applications that must enter XIP mode immediately after power-up, nonvolatile configuration register bit settings can enable XIP as the default mode.

Execute-in-place (XIP) mode allows the memory to be Read by sending an address to the device and then receiving the data on one, two, or four pins in parallel, depending on the customer requirements. XIP mode offers maximum flexibility to the application, saves instruction overhead, and reduces random access time.

Activate or Terminate XIP Using Volatile Configuration Register:

Applications that boot in SPI and must switch to XIP use the volatile configuration register. XIP provides faster memory Read operations by requiring only an address to execute, rather than a instruction code and an address.

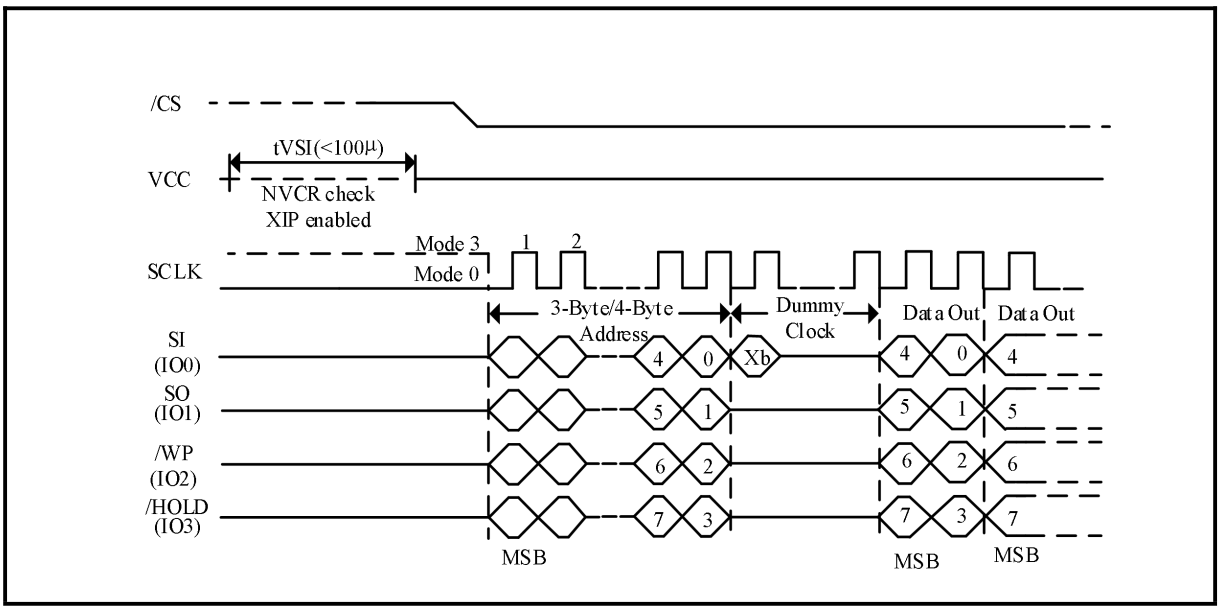
To activate XIP requires two steps. First, enable XIP by setting volatile configuration register bit 3 to 0. Next, drive the XIP confirmation bit to 0 during the next Fast Read operation. XIP is then active. Once in XIP, any instruction that occurs after /CS is toggled requires only address bits to execute; a instruction code is not necessary, and device operations use the SPI protocol that is enabled. XIP is terminated by driving the XIP confirmation bit to 1. The device automatically resets volatile configuration register bit 3 to 1.

Note: For devices with basic XIP, indicated by a part number feature set digit of 2 or 4, it is not necessary to set the volatile configuration register bit 3 to 0 to enable XIP. Instead, it is enabled by setting the XIP confirmation bit to 0 during the first dummy clock cycle after any FAST READ command.

Activate or Terminate XIP Using Nonvolatile Configuration Register:

Applications that must boot directly in XIP use the nonvolatile configuration register. To enable a device to power-up in XIP using the nonvolatile configuration register, set nonvolatile configuration register bits [11:9]. Settings vary according to protocol, as explained in the Nonvolatile Configuration Register section. Because the device boots directly in XIP, after the power cycle, no instruction code is necessary. XIP is terminated by driving the XIP confirmation bit to 1.

Figure 8. XIP Mode Directly After Power-On



Note:

1. Xb is the XIP confirmation bit and should be set as follows: 0 to keep XIP state; 1 to exit XIP mode and return to standard Read mode.

Confirmation Bit Settings Required to Activate or Terminate XIP: The XIP confirmation bit setting activates or terminates XIP after it has been enabled or disabled. This bit is the value on SI during the first dummy clock cycle in the Fast Read operation. In dual I/O XIP mode, the value of IO1 during the first dummy clock cycle after the addresses is always "Don't Care". In quad I/O XIP mode, the values of IO3, IO2 and IO1 during the first dummy clock cycle after the addresses are always "Don't Care".

Table 18: XIP Confirmation Bit

Bit Value	Description
0	Activates XIP: While this bit is 0, XIP remains activated.
1	Terminates XIP: When this bit is set to 1, XIP is terminated and the device returns to SPI.

Table 19: Effects of Running XIP in Different Protocols

Protocol	Effect
Extended I/O and Dual I/O	In a device with a dedicated part number where RST# is enabled, a LOW pulse on that pin resets XIP and the device to the state it was in previous to the last power-up, as defined by the nonvolatile configuration register.
Dual I/O	Values of SO during the first dummy clock cycle are "Don't Care".
Quad I/O[1]	Values of IO[3:1] during the first dummy clock cycle are "Don't Care". In a device with a dedicated part number, it is only possible to reset memory when the device is deselected.

Note:

1. In a device with a dedicated part number where RST# is enabled, a LOW pulse on that pin resets XIP and the device to the state it was in previous to the last power-up, as defined by the nonvolatile configuration register only when the device is deselected.

Terminating XIP After a Controller and Memory Reset:

The system controller and the device can become out of synchronization if, during the life of the application, the system controller is reset without the device being reset. In such a case, the controller can reset the memory to power-on reset if the memory has reset functionality. IO0 (SI) and IO3 (HOLD) equal to 1 for the situations listed below:

- 7 clock cycles within /CS Low (/CS becomes High before 8th clock cycle)
- + 9 clock cycles within /CS Low (/CS becomes High before 10th clock cycle)
- + 13 clock cycles within /CS Low (/CS becomes High before 14th clock cycle)
- + 17 clock cycles within /CS Low (/CS becomes High before 18th clock cycle)
- + 25 clock cycles within /CS Low (/CS becomes High before 26th clock cycle)
- + 33 clock cycles within /CS Low (/CS becomes High before 34th clock cycle)

These sequences cause the controller to set the XIP confirmation bit to 1, thereby terminating XIP. However, it does not reset the device or interrupt Program/Erase operations that may be in progress. After terminating XIP, the controller must execute Reset Enable and Reset Memory to implement a software reset and reset the device.

6. Device Identification

The device can use the Read ID and Multiple I/O Read ID instruction to access the device identification, these identification include Manufacturer ID, Device ID and Unique ID, among which Unique ID can only be accessed by the Read ID instruction. The returned data bytes provide the information as shown in the below table.

Table 20. Read ID Data Out

Size (Bytes)	Name	Content Value	Assigned by
1	**Manufacturer ID**		JEDEC
2	**Device ID**		
	Memory Type		Manufacturer
	Memory Capacity	21H (1Gb)	
17	**Unique ID**		
	1 Byte: Length of data to follow	10H	Factory
	2 Bytes: Extended device ID and device configuration information	ID and information such as uniform architecture, and HOLD or RESET functionality	
	14 Bytes: Customized factory data	Optional	

Note:
1. The 17 bytes of information in the unique ID is Read by the READ ID instruction, but cannot be Read by the Multiple I/O Read ID instruction.

Table 21: Extended Device ID, First Byte

Bit 7	Bit 6	Bit 5	Bit 4[1]	Bit 3	Bit 2	Bit 1	Bit 0
Reser-ved	Reser-ved	0 = Standard BP scheme	Volatile configuration register bit setting: 0 = BY Technology XIP 1 = Basic XIP	/HOLD or /RESET: 0 = HOLD 1 = RESET	Addressing: 0 = by byte	Architecture: 00 = Uniform	

Note:
1. For more information, contact the factory.

7. Instructions Description

All instructions, addresses and data are shifted in and out of the device, beginning with the most significant bit on the first rising edge of SCLK after /CS is driven low. Then, the one byte instruction code must be shifted in to the device, each bit being latched on the rising edges of SCLK.

See ***Table 22***, every instruction sequence starts with a one-byte instruction code. Depending on the instruction, this might be followed by address bytes, or by data bytes, or by both or none. /CS must be driven high after the last bit of the instruction sequence has been shifted in. For the instruction of Read, Fast Read, Read Status Register, and Read Device ID, the shifted-in instruction sequence is followed by a data out sequence. /CS can be driven high after any bit of the data-out sequence is being shifted out.

For the instruction of Page Program, Subsector Erase, Sector Erase, Die Erase, Write Status Register, Write Enable, Write Disable instruction, etc. /CS must be driven high exactly at a byte boundary, otherwise the instruction is rejected, and is not executed. That is /CS must drive high when the number of clock pulses after /CS being driven low is an exact multiple of eight. For Page Program, if at any time the input byte is not a full byte, nothing will happen and WEL will not be reset.

Table 22. Instruction Set Table

Note 1 applies to entire table

Instruction	Code	Extended	Dual I/O	Quad I/O	Data Bytes	Note
Register Operations						
Write Enable	06H	Yes	Yes	Yes	0	2
Write Disable	04H	Yes	Yes	Yes	0	2
Read Status Register	05H	Yes	Yes	Yes	1 to ∞	2
Write Status Register	01H	Yes	Yes	Yes	1	2,13,15
Read Lock Register	E8H	Yes	Yes	Yes	1 to ∞	4
Write Lock Register	E5H	Yes	Yes	Yes	1 to ∞	4, 13
Read Flag Status Register	70H	Yes	Yes	Yes	1 to ∞	2
Clear Flag Status Register	50H	Yes	Yes	Yes	0	2
Read Nonvolatile Configuration Register	B5H	Yes	Yes	Yes	2	2
Write Nonvolatile Configuration Register	B1H	Yes	Yes	Yes	2	2,13,15
Register Operations						

Instruction	Code	Extended	Dual I/O	Quad I/O	Data Bytes	Note
Read Volatile Configuration Register	85H	Yes	Yes	Yes	1 to ∞	2
Write Volatile Configuration Register	81H	Yes	Yes	Yes	1	2, 13
Read Enhanced Volatile Configuration Register	65H	Yes	Yes	Yes	1 to ∞	2
Write Enhanced Volatile Configuration Register	61H	Yes	Yes	Yes	1	2, 13
Read Extended Address Register	C8H	Yes	Yes	Yes	0	2
Write Extended Address Register	C5H	Yes	Yes	Yes	0	2, 13
Enter 4-BYTE Address Mode	B7H	Yes	Yes	Yes	0	2, 13
EXIT 4-BYTE Address Mode	E9H	Yes	Yes	Yes	0	2, 13
Reset Enable	66H	Yes	Yes	Yes	0	2
Reset Memory	99H	Yes	Yes	Yes	0	2
Read Operations						
Read	03H	Yes	No	No	1 to ∞	4
Fast Read	0BH	Yes	Yes	Yes	1 to ∞	5
Dual Output Fast Read	3BH	Yes	Yes	No	1 to ∞	5
Dual Input/Output Fast Read	BBH	Yes	Yes	No	1 to ∞	5,11
Quad Output Fast Read	6BH	Yes	No	Yes	1 to ∞	5
Quad Input/Output Fast Read	EBH	Yes	No	Yes	1 to ∞	5,12
Fast Read-DTR	0DH	Yes	Yes	Yes	1 to ∞	6
Dual Output Fast Read-DTR	3DH	Yes	Yes	No	1 to ∞	6
Dual Input/Output Fast Read-DTR	BDH	Yes	Yes	No	1 to ∞	6
Quad Output Fast Read-DTR	6DH	Yes	No	Yes	1 to ∞	6
Quad Input/Output Fast Read-DTR	EDH	Yes	No	Yes	1 to ∞	7

Instruction	Code	Extended	Dual I/O	Quad I/O	Data Bytes	Note
4-Byte Read	13H	Yes	No	No	1 to ∞	8
4-Byte Fast Read	0CH	Yes	Yes	Yes	1 to ∞	9
4-Byte Dual Output Fast Read	3CH	Yes	Yes	No	1 to ∞	9
4-Byte Dual Input/ Output Fast Read	BCH	Yes	Yes	No	1 to ∞	9, 11
4-Byte Quad Output Fast Read	6CH	Yes	No	Yes	1 to ∞	9
4 Byte Quad Input/ Output Fast Read	ECH	Yes	No	Yes	1 to ∞	10,12
Identification Operations						
Read ID	9E/9FH	Yes	No	No	1 to 20	2
Multiple I/O Read ID	AFH	No	Yes	Yes	1 to 3	2
Read Serial Flash Discovery Parameter	5AH	Yes	Yes	Yes	1 to ∞	3
Program and Erase Operations						
Page Program	02H	Yes	Yes	Yes	1 to 256	4,13,14
Dual Input Fast Program	A2H	Yes	Yes	No	1 to 256	4,13,14
Extended Dual Input Fast Program	D2H	Yes	Yes	No	1 to 256	4,11,13,14
Quad Input Fast Program	32H	Yes	No	Yes	1 to 256	4,13,14
Extended Quad Input Fast Program	12H	Yes	No	Yes	1 to 256	4,12,13,14
Subsector Erase	20H	Yes	Yes	Yes	0	4, 13,14
Sector Erase	D8H	Yes	Yes	Yes	0	4,13, 14
Die Erase	C4H	Yes	Yes	Yes	0	4,13, 14
Program/Erase Resume	7AH	Yes	Yes	Yes	0	2,13,14
Program/Erase Suspend	75H	Yes	Yes	Yes	0	2,13,14
OTP Operations						

Instruction	Code	Extended	Dual I/O	Quad I/O	Data Bytes	Note
Read OTP Array	4BH	Yes	Yes	Yes	1 to 64	5
Program OTP Array	42H	Yes	Yes	Yes	1 to 64	4,13,14

Note:

1. Yes in the protocol columns indicates that the instruction is supported and has the same functionality and instruction sequence as other instructions marked Yes.
2. Address bytes = 0. Dummy clock cycles = 0.
3. Address bytes = 3. Dummy clock cycles default = 8.
4. Address bytes default = 3; address bytes = 4 (extended address). Dummy clock cycles = 0.
5. Address bytes default = 3; address bytes = 4 (extended address). Dummy clock cycles default = 8. Dummy clock cycles default = 10 (when quad SPI protocol is enabled). Dummy clock cycles are configurable by the user.
6. Address bytes default = 3; address bytes = 4 (extended address). Dummy clock cycles default = 6. Dummy clock cycles default = 8 when quad SPI protocol is enabled. Dummy clock cycles are configurable by the user.
7. Address bytes default = 3; address bytes = 4 (extended address). Dummy clock cycles default = 8. Dummy clock cycles are configurable by the user.
8. Address bytes = 4. Dummy clock cycles = 0.
9. Address bytes = 4. Dummy clock cycles default = 8. Dummy clock cycles default = 10 (when quad SPI protocol is enabled). Dummy clock cycles are configurable by the user.
10. Address bytes = 4. Dummy clock cycles default = 10. Dummy clock cycles is configurable by the user.
11. When the device is in dual SPI protocol, the instruction can be entered with any of these three codes. The different codes enable compatibility between dual SPI and extended SPI protocols.
12. When the device is in quad SPI protocol, the instruction can be entered with any of these three codes. The different codes enable compatibility between quad SPI and extended SPI protocols.
13. The Write Enable instruction must be issued first before this instruction can be executed.
14. Requires the Read Flag Status Register instruction being issued with at least one byte output. (After code, at least 8 clock pulses in extended SPI, 4 clock pulses in dual I/O SPI, and 2 clock pulses in quad I/O SPI.) The cycle is not complete until bit 7 of the flag status register outputs 1.
15. The end of operation can be detected by means of a Read Flag Status Register instruction being issued four times, /CS toggled between each instruction execution, and bit 7 of the flag status register outputs 1 for all four Read operations.

Table 23. Instructions that need to send the Write Enable/Write Enable for Status Register instruction

Mode	Instruction		Write
Extended SPI/ DIO-SPI/ QIO-SPI	Write Status Register	01H	06H
	Write Nonvolatile Configuration Register	B1H	06H
	Write Volatile Configuration Register	81H	06H
	Write Enhanced Volatile Configuration Register	61H	06H
	Write Extended Address Register	C5H	06H
	Write Lock Register	E5H	06H
	Enter 4-Byte Address Mode	B7H	06H
	Exit 4-Byte Address Mode	E9H	06H
	Page Program	02H	06H
	Subsector Erase	20H	06H
	Sector Erase	D8H	06H
	Die Erase	C4H	06H
	Program OTP Array	42H	06H
Extended SPI/ DIO-SPI	Dual Input Fast Program	A2H	06H
	Extended Dual Input Fast Program	D2H	06H
Extended SPI/QIO-SPI	Quad Input Fast Program	32H	06H
	Extended Quad Input Fast Program	12H	06H

7.1 Configuration and Status Instructions

7.1.1 Write Enable (06H)

See ***Figure 9 -Figure 10***，the Write Enable instruction is for setting the Write Enable Latch bit. The Write Enable Latch bit must be set before every Program, Erase, Write, Enter 4-Byte Address Mode, and Exit 4-Byte Address Mode instruction. The Write Enable instruction sequence: /CS goes low sending the Write Enable instruction /CS goes high.

If /CS is not driven high after the instruction code has been latched in, the instruction is not executed, flag status register error bits are not set, and the write enable latch remains cleared to its default setting of 0.

Figure 9. Write Enable Sequence Diagram (Extended SPI Mode)

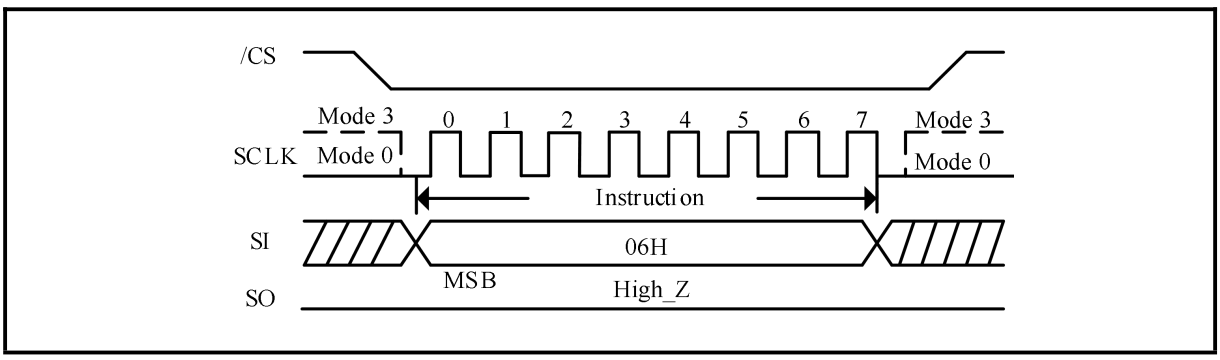
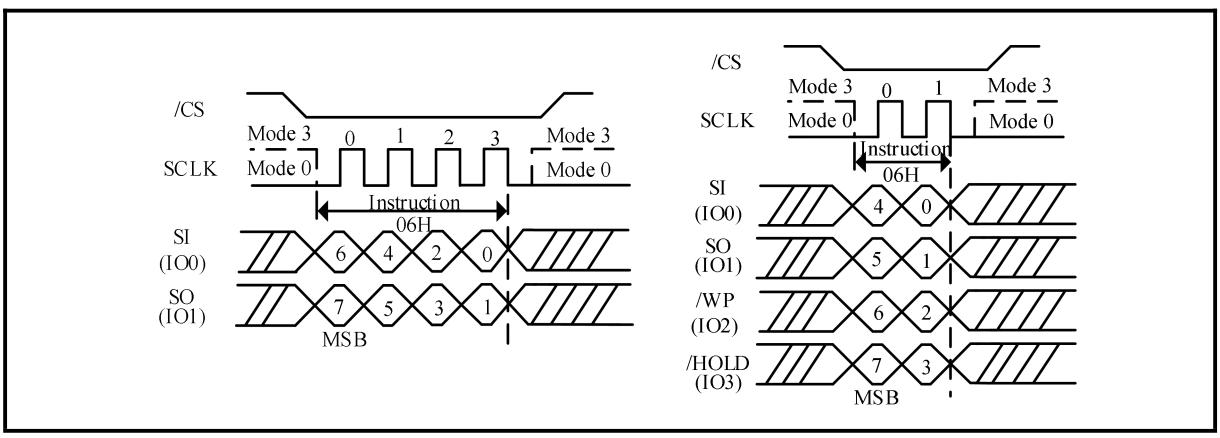


Figure 10. Write Enable Sequence Diagram (Dual/Quad I/O Mode)



7.1.2 Write Disable (04H)

See ***Figure 11-Figure 12***, the Write Disable instruction is for resetting the Write Enable Latch bit or invalidate the Write Enable for Volatile Status Register instruction. The Write Disable instruction sequence: /CS goes low -> sending the Write Disable instruction -> /CS goes high. The Write Enable Latch bit is reset by following condition: Power-up and upon completion of Program, Erase, Enter 4-Byte Address Mode , Exit 4-Byte Address Mode instruction, Program OTP Array and Reset Memory instructions.

If /CS is not driven High after the instruction code has been latched in, the instruction is not executed, flag status register error bits are not set, and the write enable latch remains set to 1.

Note: In case of a protection error, write disable will not clear the write enable latch. In this situation, a Clear Flag Status Register instruction must be issued to clear both flags.

Figure 11. Write Disable Sequence Diagram (Extended SPI Mode)

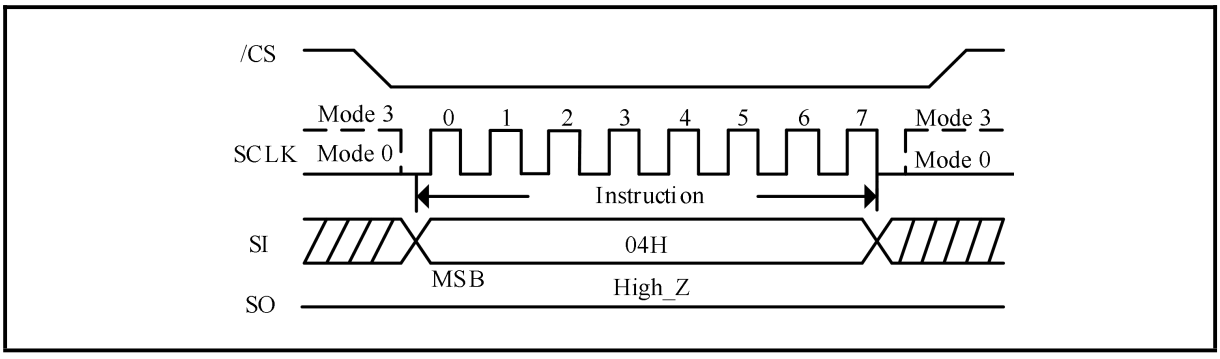
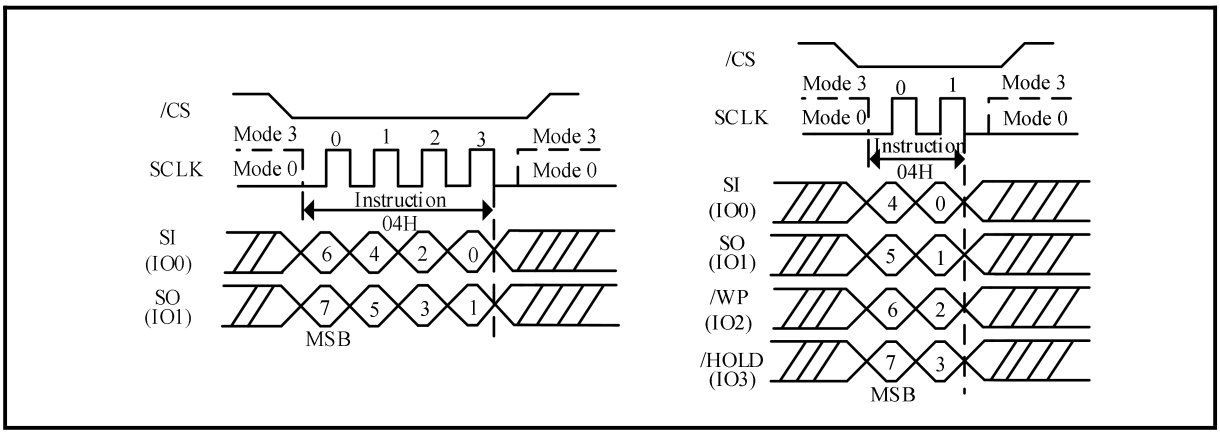


Figure 12. Write Disable Sequence Diagram (Dual/Quad I/O Mode)



7.1.3 Read Status Register (05H)

See ***Figure 13-Figure 14***, the Read Status Register instruction is for Reading the Status Register. The Status Register may be Read at any time, even while a Program, Erase or Write Status Register cycle is in progress. The operation is terminated by driving /CS High at any time during data output. The status register can be Read continuously and at any time, including during a Program, Erase, or Write operation.

If one of these operations is in progress, checking the write in progress bit or Program or erase controller bit is recommended before executing the instruction.

Figure 13. Read Status Register Sequence Diagram (Extended SPI Mode)

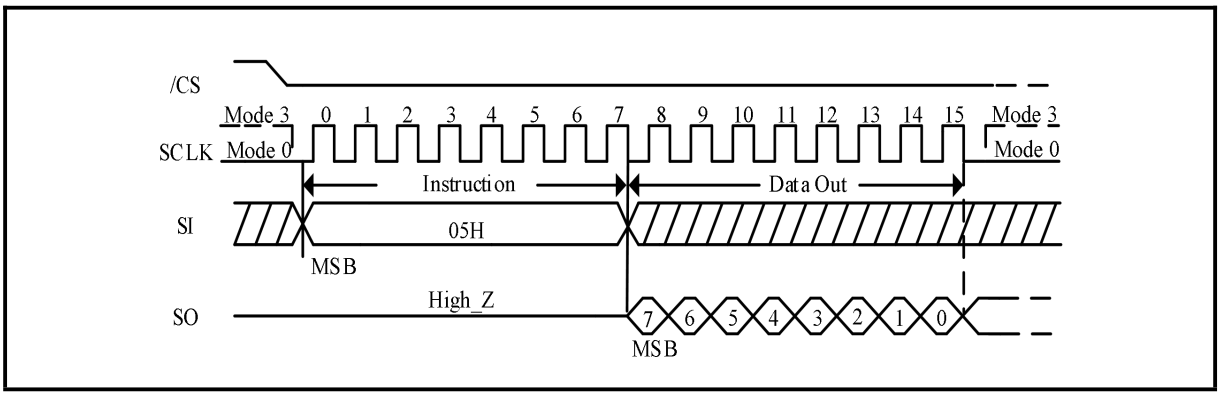
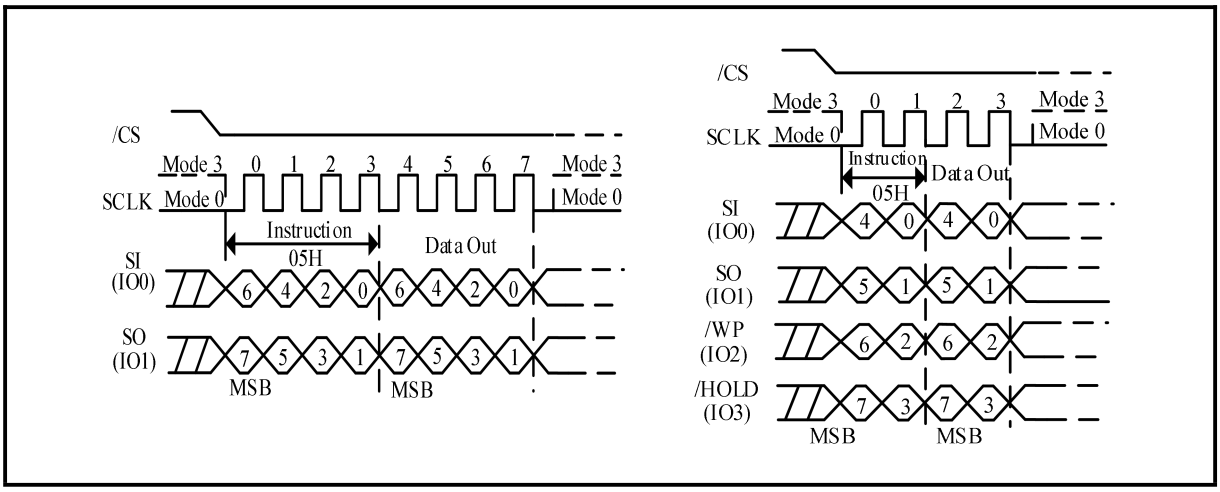


Figure 14. Read Status Register Sequence Diagram (Dual/Quad I/O Mode)



7.1.4 Write Status Register (01H)

To issue a Write Status Register instruction (see the ***Figure 15-Figure 16***), the Write Enable instruction must be executed to set the Write Enable Latch bit to 1. The Write Status Register instruction is used to write new values to status register bits 7:2, enabling software data protection.The status register can also be combined with the /W/VPP signal to provide hardware data protection. The Write Status Register instruction has no effect on status register bits 1:0.

The sequence of issuing Write Status Register instruction is: /CS goes low→ sending Write Status Register instruction code→ Status Register data on SI (For Dual SPI protocol data on IO0-IO1,Quad SPI protocol data on IO0-IO3)→/CS goes high. When /CS is driven high, the operation, which is self-timed, is initiated; its duration is tW.

When the operation is in progress, the Program or Erase controller bit of the Flag Status Register is set to 0. To obtain the operation status, the Flag Status Register must be polled four times, with /CS toggled twice in between instructions. When the operation completes, the Program or Erase controller bit is cleared to 1. The end of operation can be detected when the Flag Status Register outputs the Program or Erase controller bit to 1 each of the four times. When the maximum time is achieved (see AC Electrical Characteristics), polling the flag status register four times is not required.

Figure 15. Write Status Register Sequence Diagram (Extended SPI Mode)

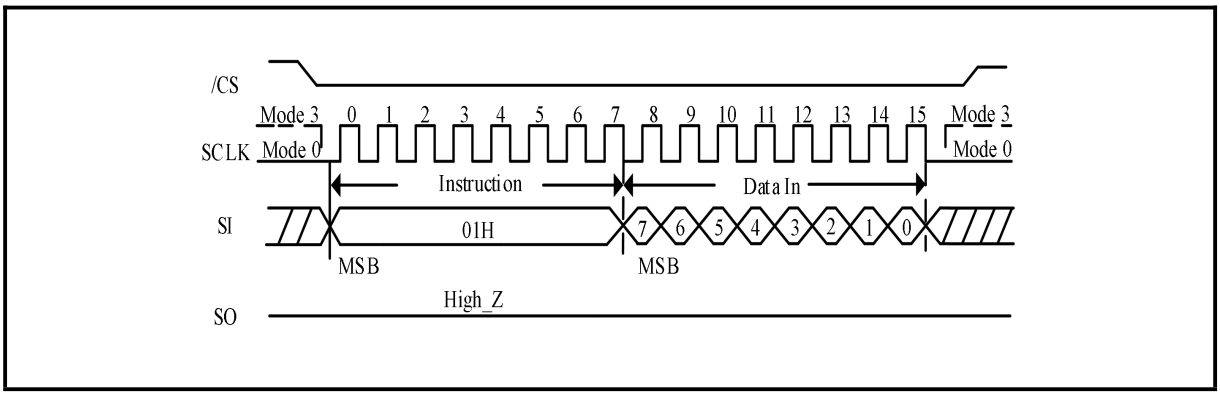
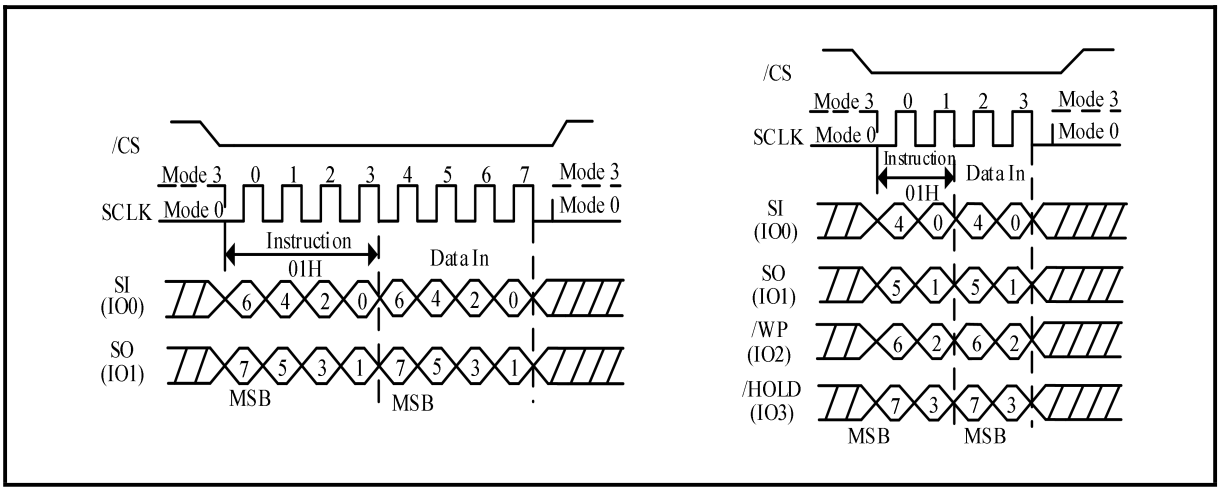


Figure 16. Write Status Register Sequence Diagram (Dual/Quad I/O Mode)



7.1.5 Read Flag Status Register (70H)

See ***Figure 17-Figure 18***, the Read Flag Status Register instruction is for Reading the Flag Status Register. The flag status register must be Read any time a Program, Erase, or Suspend/Resume instruction is issued, or after a Reset instruction while device is busy. The cycle is not complete until bit 7 of the flag status register outputs 1. Refer to Instruction Definitions for more information. The operation is terminated by driving /CS High at any time during data output. The status register can be Read continuously and at any time, including during a Program, Erase, or Write operation.

If Read Flag Status Register operations is in progress, checking the Write in Progress bit or Program or Erase controller bit is recommended before executing the instruction.

Note: The end of an operation (such as a power-up, Write Status Register, or Write Nonvolatile Configuration Register) is determined by issuing the Read Flag Status Register instruction once for each die in the device, with /CS toggled between instructions until each die is Ready. Bit 7 of the flag status register outputs a value of 1 each time.

Figure 17. Read Flag Status Register Sequence Diagram (Extended SPI Mode)

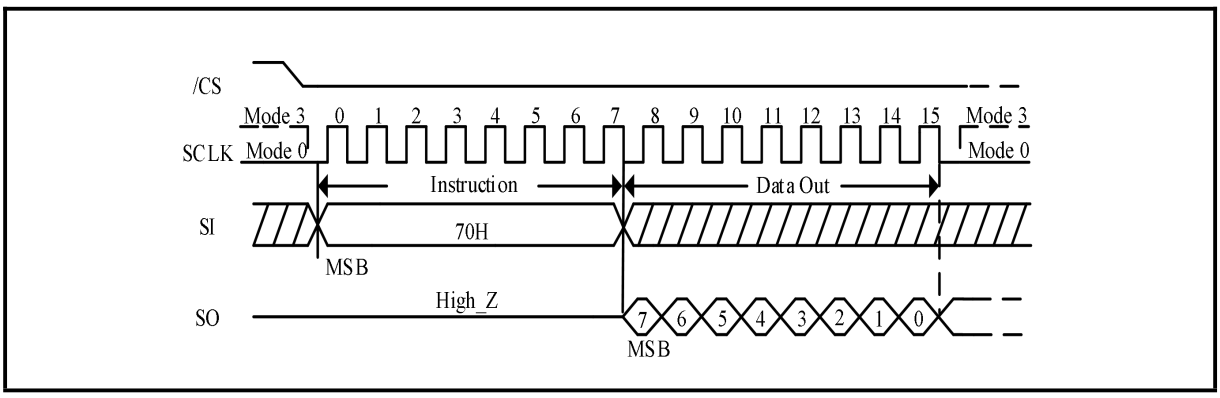
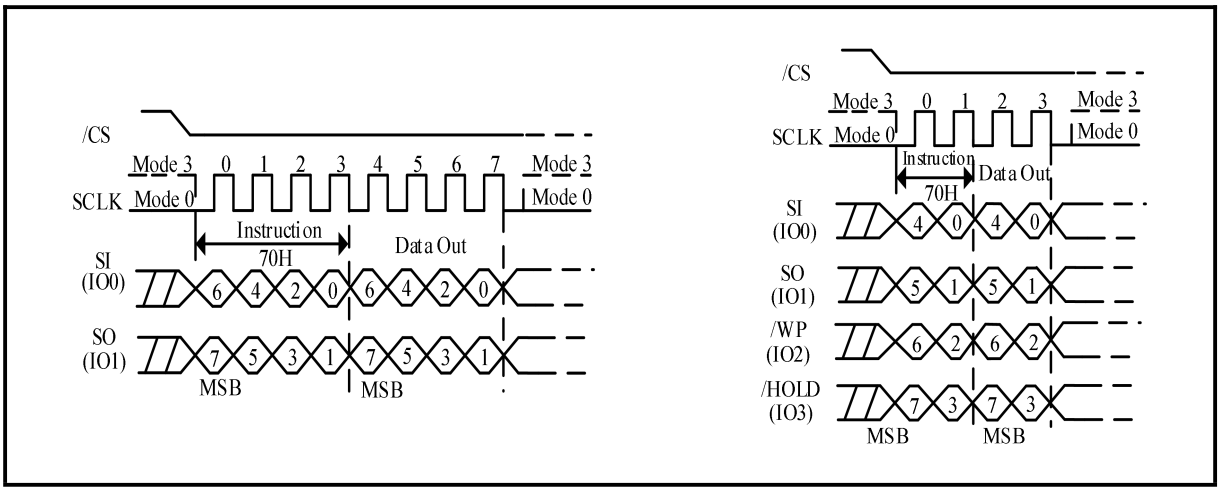


Figure 18. Read Flag Status Register Sequence Diagram (Dual/Quad I/O Mode)



7.1.6 Read Nonvolatile Configuration Register (B5H)

To execute a Read Nonvolatile Configuration Register instruction (see the ***Figure 19-Figure 20***), /CS is driven Low. For extended SPI protocol, the instruction code is input on SI, and output on SO. For dual SPI protocol, the instruction code is input on IO0-IO1, and output on IO0-IO1. For quad SPI protocol, the instruction code is input on IO0-IO3, and is output on IO0-IO3. The operation is terminated by driving /CS High at any time during data output. The operation will output data starting from the least significant byte.

The nonvolatile configuration register can be Read continuously. After all 16 bits of the register have been Read, a 0 is output. All reserved fields output a value of 1.

Figure 19. Read Nonvolatile Configuration Register Sequence Diagram (SPI Mode)

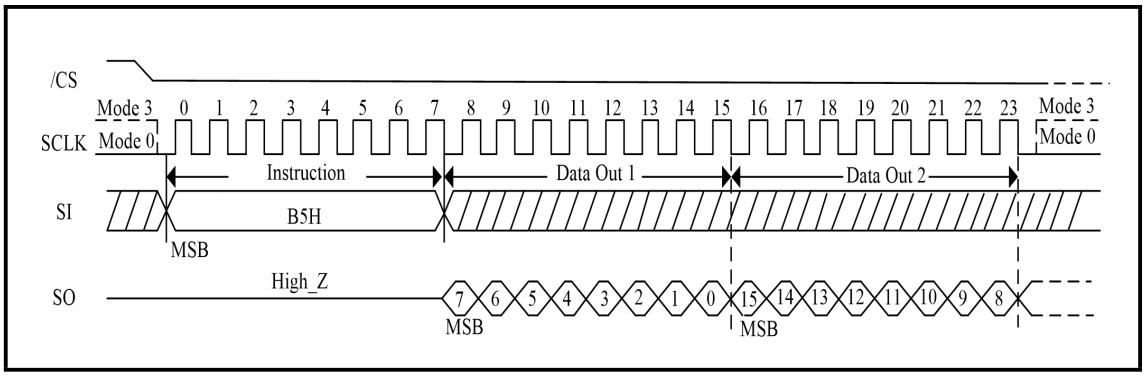
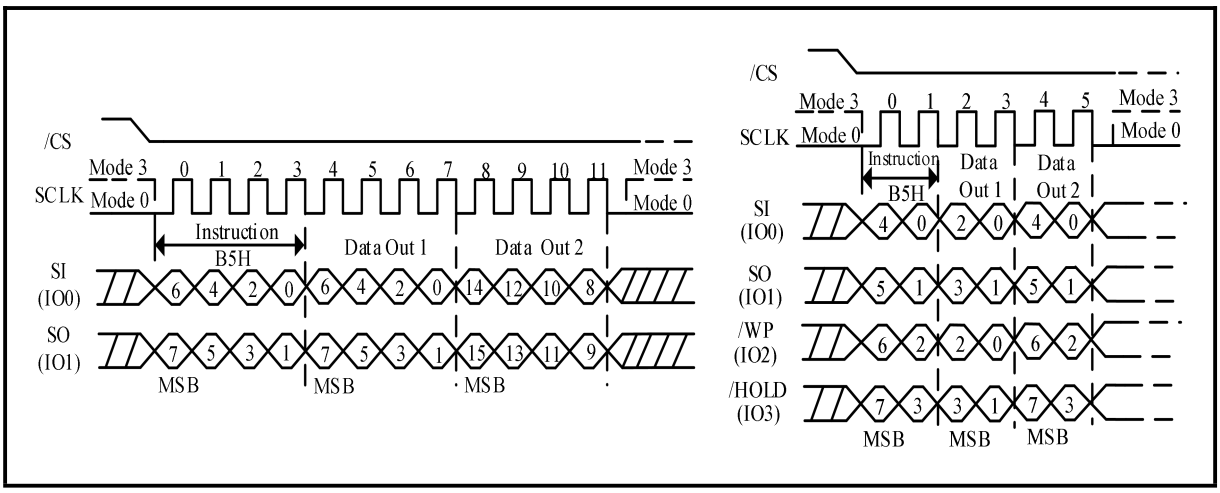


Figure 20. Read Nonvolatile Configuration Register (Dual/Quad I/O Mode)



7.1.7 Write Nonvolatile Configuration Register (B1H)

To execute the Write Nonvolatile Configuration Register instruction (see the ***Figure 21-Figure 22***), the Write Enable instruction must be executed to set the Write Enable Latch bit to 1. /CS is driven low and held low until the 16th bit of the last data byte has been latched in, after which it must be driven high. For extended SPI protocol, the instruction code is input on SI, followed by two data bytes. For dual SPI protocol, the instruction code is input on IO0-IO1, followed by the data bytes. For quad SPI protocol, the instruction code is input on IO0-IO3, followed by the data bytes. When /CS is driven high, the operation, which is self-timed, is initiated; its duration is tWNVCR.

When the operation is in progress, the Program or Erase controller bit of the flag status register is set to 0. To obtain the operation status, the Flag Status Register must be polled four times, with /CS toggled twice in between instructions. When the operation completes, the Program or Erase controller bit is cleared to 1. The end of operation can be detected when the Flag Status Register outputs the Program or Erase controller bit to 1 each of the four times. When the maximum time is achieved (see AC Electrical Characteristics), polling the flag status register four times is not required. The operation requires data being sent starting from least significant byte. For this instruction, the data in consists of two bytes.

Figure 21. Write Nonvolatile Configuration Register (Extended SPI Mode)

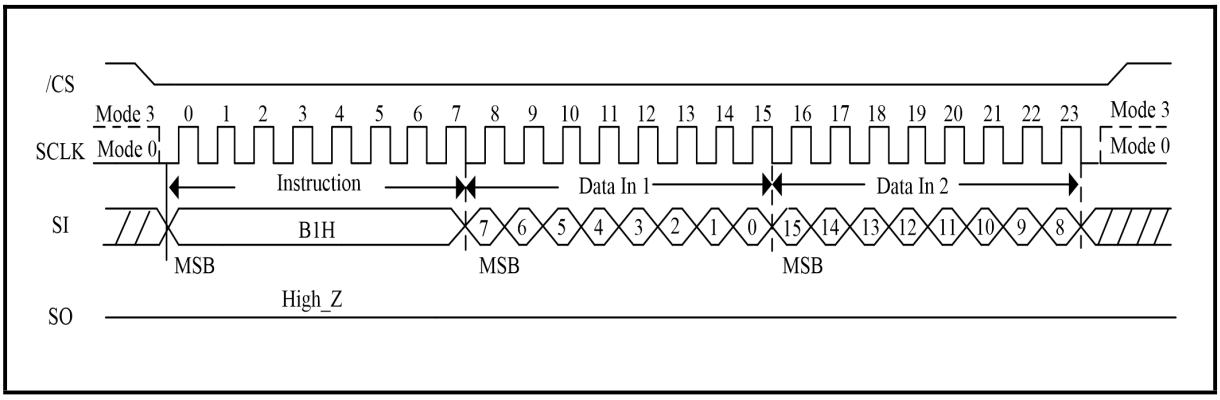
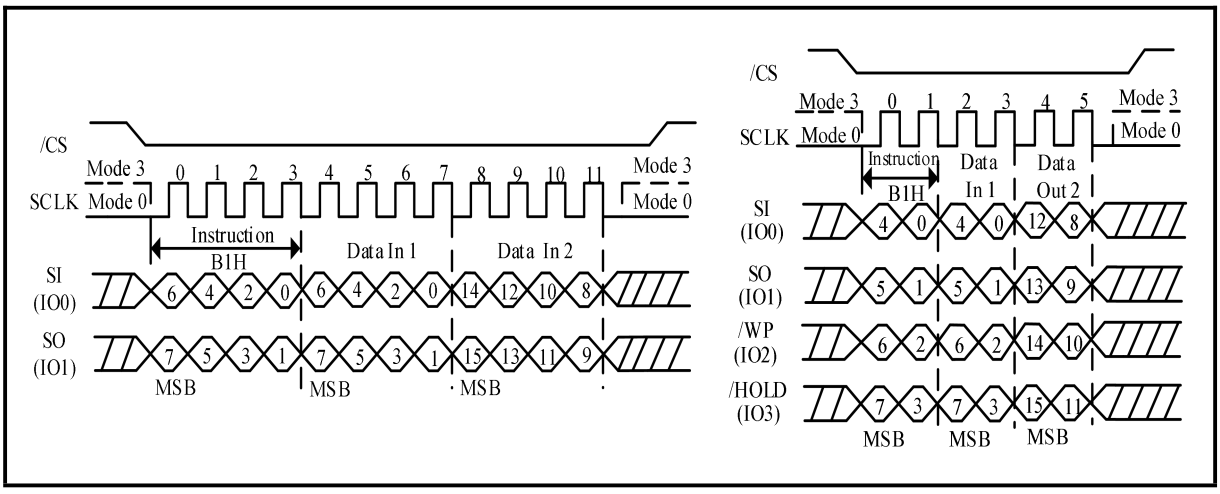


Figure 22. Write Nonvolatile Configuration Register (Dual/Quad I/O Mode)



7.1.8 Read Volatile or Enhanced Volatile Configuration Register (85/65H)

See ***Figure 23-Figure 24***, the Read Volatile Configuration Register instruction or a Read Enhanced Volatile Configuration Register instruction is for Reading Volatile or Enhanced Volatile Configuration Register. When the register is Read continuously, the same byte is output repeatedly.

The sequence of issuing Read Volatile or Enhanced Volatile Configuration Register instruction is: /CS goes low→ sending Read Volatile or Enhanced Volatile Configuration Register instruction code→ Status Register data on SI(For Dual SPI protocol data on IO0-IO1, Quad SPI protocol data on IO0-IO3)→/CS goes high. The operation is terminated by driving /CS High at any time during data output.

Figure 23. Read Volatile or Enhanced Volatile Configuration Register (Extended SPI Mode)

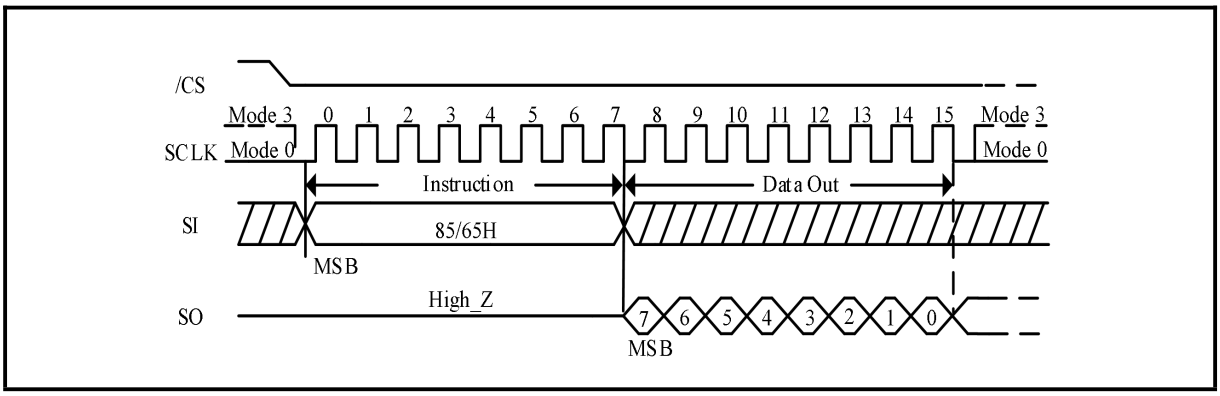
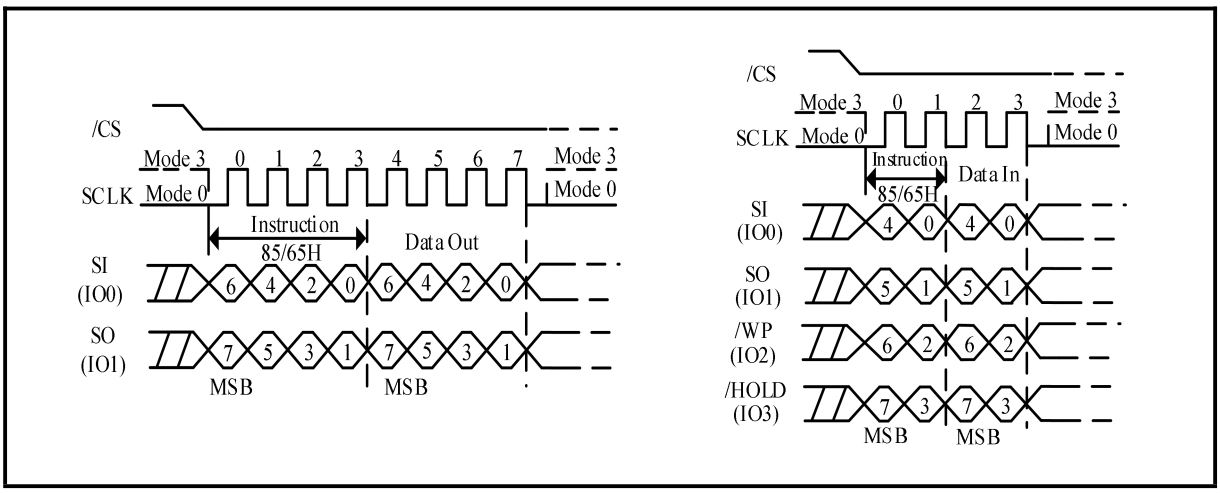


Figure 24. Read Volatile or Enhanced Volatile Configuration Register (Dual/Quad I/O Mode)



7.1.9 Write Volatile or Enhanced Volatile Configuration Register (81/61H)

To execute a Write Volatile Configuration Register instruction or a Write Enhanced Volatile Configuration Register instruction (see the ***Figure 25-Figure 26***), the Write Enable instruction must be executed to set the write enable latch bit to 1. /CS is driven low and held low until the eighth bit of the last data byte has been latched in, after which it must be driven high. For extended SPI protocol, the instruction code is input on SI, followed by the data bytes. For dual SPI protocol, the instruction code is input on IO0-IO1, followed by the data bytes. For quad SPI protocol, the instruction code is input on IO0-IO3, followed by the data bytes.

Because register bits are volatile, change to the bits is immediate. After the data is latched in, /CS must be driven high. Reserved bits are not affected by this instruction.

Figure 25. Write Nonvolatile Configuration Register (Extended SPI Mode)

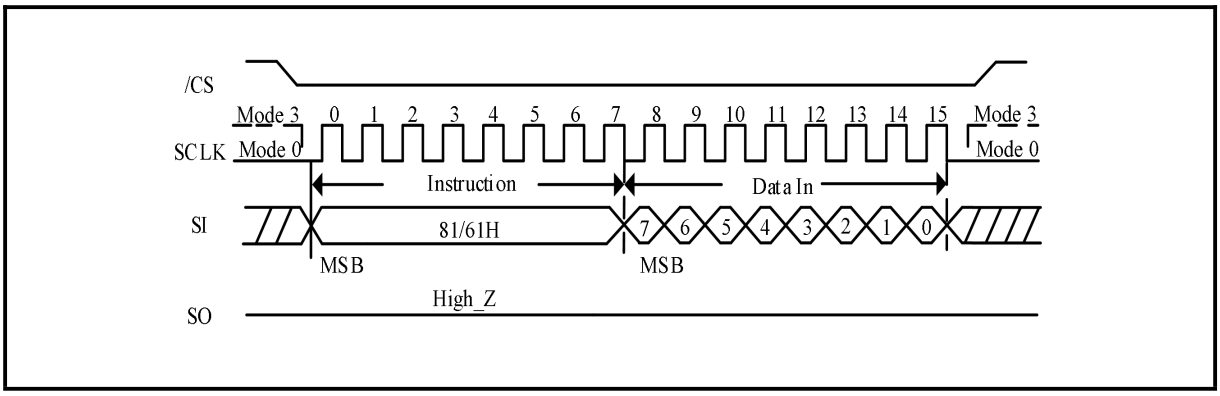
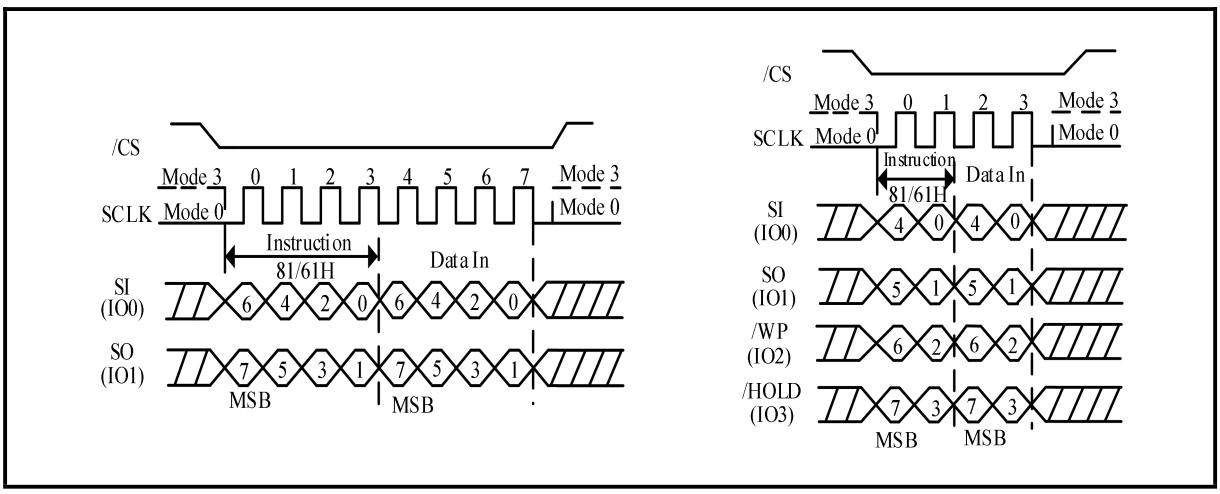


Figure 26. Write Nonvolatile Configuration Register (Dual/Quad I/O Mode)



7.1.10 Read Extended Address Register (C8H)

When the device is in the 3-Byte Address Mode, the Extended Address Register is used as the 4th address byte A[31:24] to access memory regions beyond 128Mb. See **Figure 27-*Figure 28***, to initiate a Read Extended Address Register instruction, /CS is driven low. For extended SPI protocol, the instruction code is input on SI, and output on SO. For dual SPI protocol, the instruction code is input on IO0-IO1, and output on IO0-IO1. For quad SPI protocol, the instruction code is input on IO0-IO3, and is output on IO0-IO3. The operation is terminated by driving /CS High at any time during data output. When the register is Read continuously, the same byte is output repeatedly.

Figure 27. Read Extended Address Register (Extended SPI Mode)

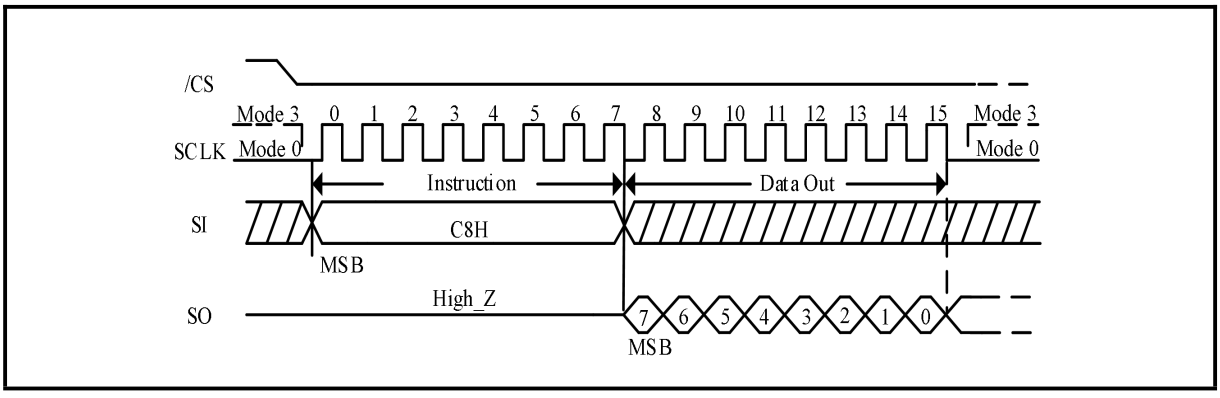
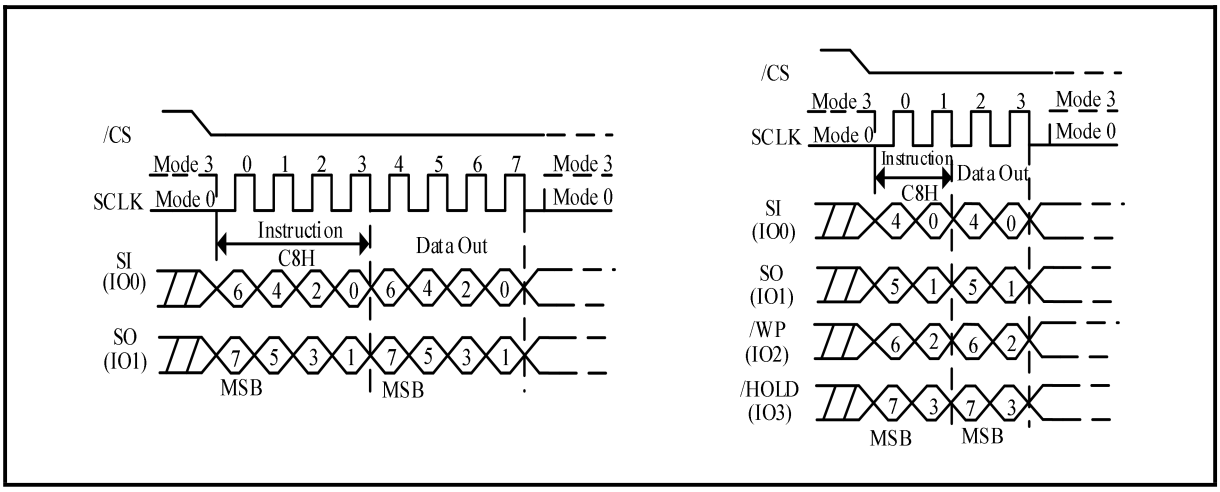


Figure 28. Read Extended Address Register (Dual/Quad I/O Mode)



7.1.11 Write Extended Address Register (C5H)

See ***Figure 29-Figure 30***, to initiate a Write Extended Address Register instruction, the Write Enable instruction must be executed to set the write enable latch bit to 1. /CS is driven low and held low until the eighth bit of the last data byte has been latched in, after which it must be driven high. For Extended SPI protocol, the instruction code is input on SI, followed by the data bytes. For dual SPI protocol, the instruction code is input on IO0-IO1, followed by the data bytes. For quad SPI protocol, the instruction code is input on IO0-IO3, followed by the data bytes.

Because register bits are volatile, change to the bits is immediate. After the data is latched in, /CS must be driven high. Reserved bits are not affected by this instruction.

Figure 29. Write Extended Address Register (Extended SPI Mode)

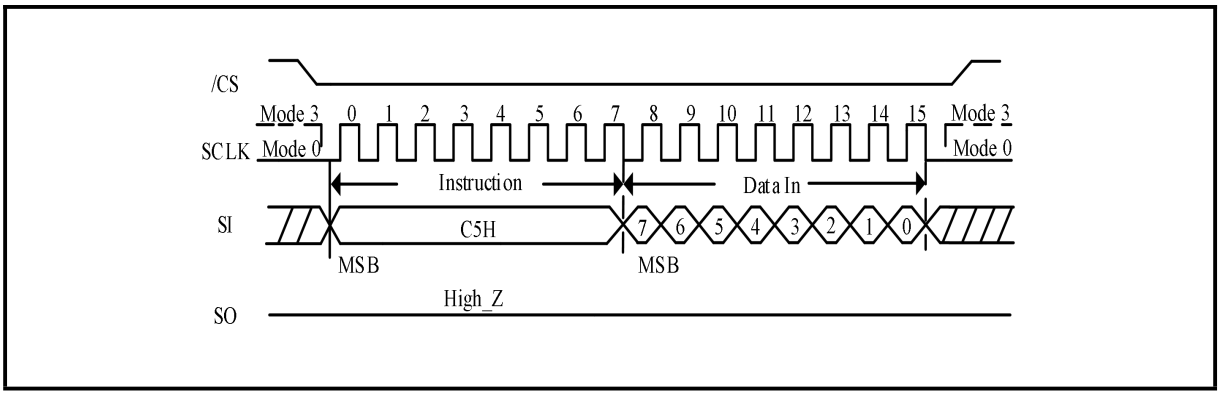
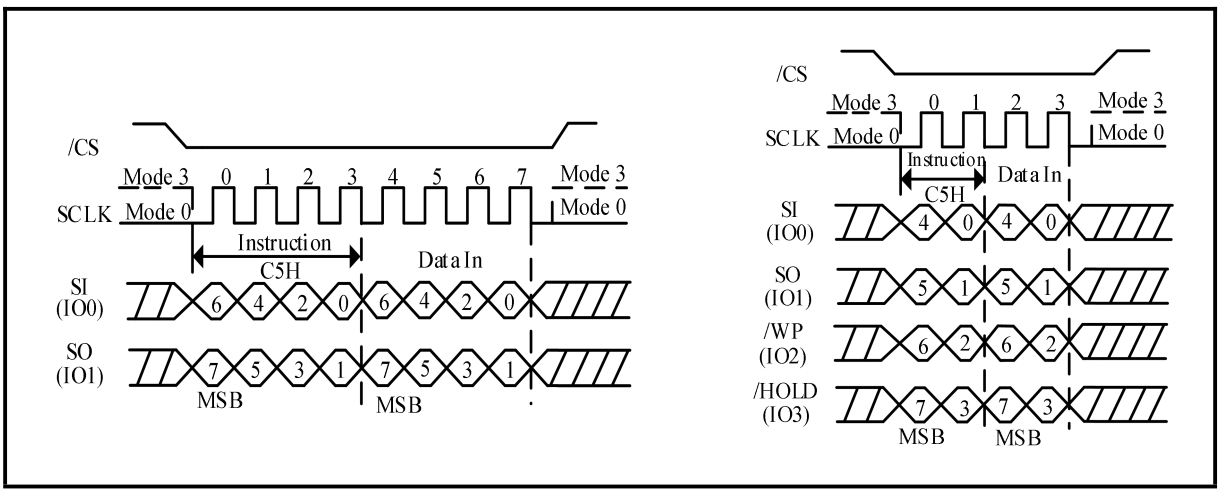


Figure 30. Write Extended Address Register (Dual I/O Mode)



7.1.12 Read Lock Register (E8H)

See ***Figure 31-Figure 33***, to execute the Read Lock Register instruction, /CS is driven low. For extended SPI protocol, the instruction code is input on SI, followed by address bytes that point to a location in the sector, and data is shifted out on SO at a maximum frequency fC during the falling edge of the clock. For dual SPI protocol, the instruction code is input on IO0-IO1, followed by address bytes that point to a location in the sector. Each address bit is latched in during the rising edge of the clock, and data is shifted out on IO0-IO1. For quad SPI protocol, the instruction code is input on SI-IO3, followed by address bytes that point to a location in the sector. Each address bit is latched in during the rising edge of the clock, and data is shifted out on IO0-IO3. The operation is terminated by driving /CS high at any time during data output.

When the register is Read continuously, the same byte is output repeatedly. Any Read Lock Register instruction that is executed while an Erase, Program, or Write cycle is in progress is rejected with no effect on the cycle in progress.

Figure 31. Read Lock Register Sequence Diagram (Extended SPI Mode)

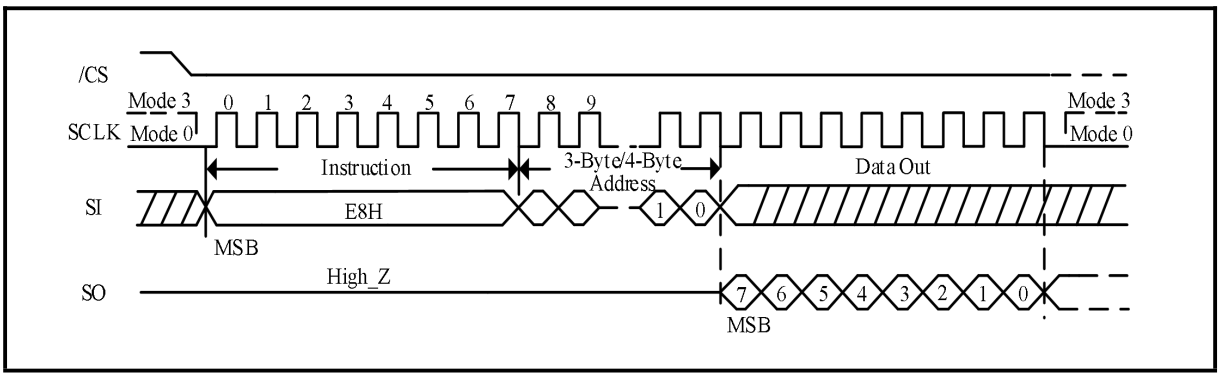


Figure 32. Read Lock Register Sequence Diagram (Dual I/O Mode)

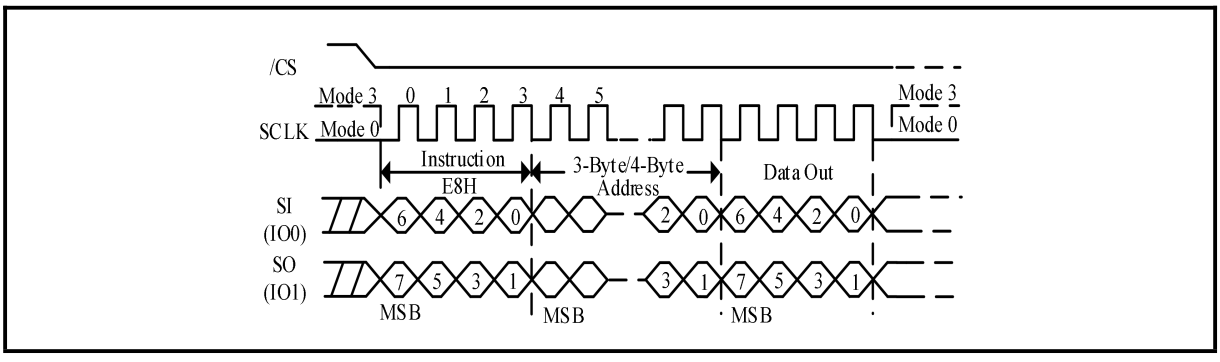
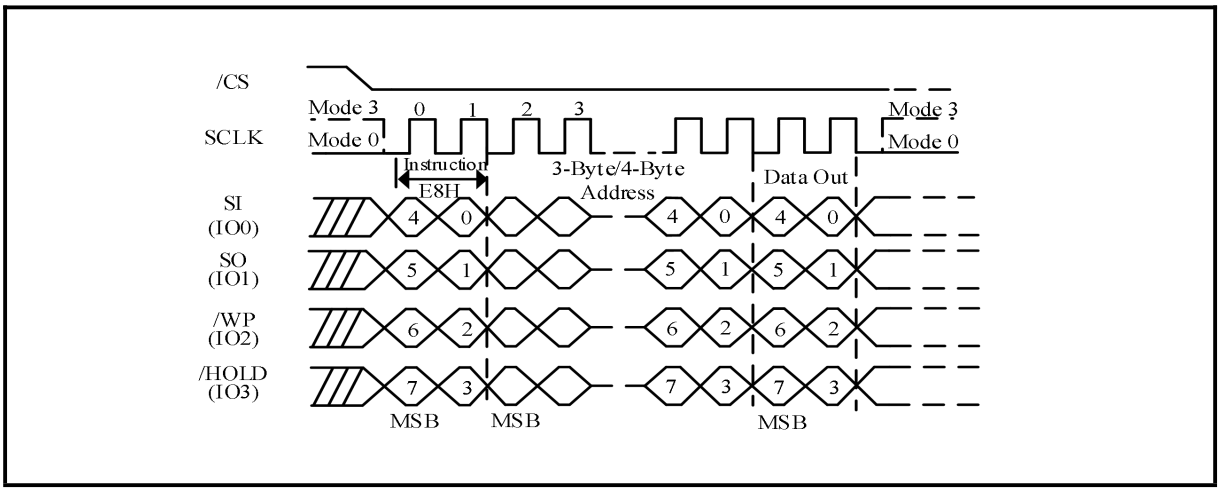


Figure 33. Read Lock Register Sequence Diagram (Quad I/O Mode)



Note:

1. Read Lock Register instruction support 3-byte address and 4-byte address mode.

7.1.13 Write Lock Register (E5H)

The Write Lock Register instruction is used to set bit 1 and bit 0 of the Lock Register, as defined in ***Table 17.*** See ***Figure 34-Figure 36***, to initiate the Write Lock Register instruction, the Write Enable instruction must be executed to set the write enable latch bit to 1. /CS is driven low and held low until the eighth bit of the last data byte has been latched in, after which it must be driven high. For extended SPI protocol, the instruction code is input on SI, followed by address bytes that point to a location in the sector, and then one data byte that contains the desired settings for lock register bits 0 and 1. For dual SPI protocol, the instruction code is input on IO0-IO1, followed by address bytes that point to a location in the sector, and then one data byte that contains the desired settings for lock register bits 0 and 1. For quad SPI protocol, the instruction code is input on IO0-IO3, followed by the data bytes, followed by address bytes that point to a location in the sector, and then one data byte that contains the desired settings for lock register bits 0 and 1.

When execution is complete, the write enable latch bit is cleared within tSHSL2 and no error bits are set. Because lock register bits are volatile, change to the bits is immediate. Write Lock Register can be executed when an Erase Suspend operation is in effect. After the data is latched in, /CS must be driven high.

Figure 34. Write lock Register Sequence Diagram (Extended SPI Mode)

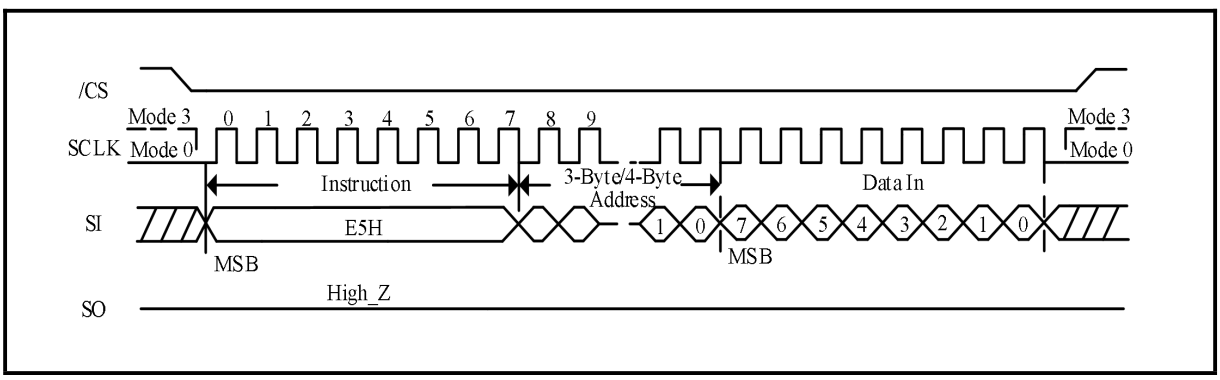


Figure 35. Write lock Register Sequence Diagram (Dual I/O Mode)

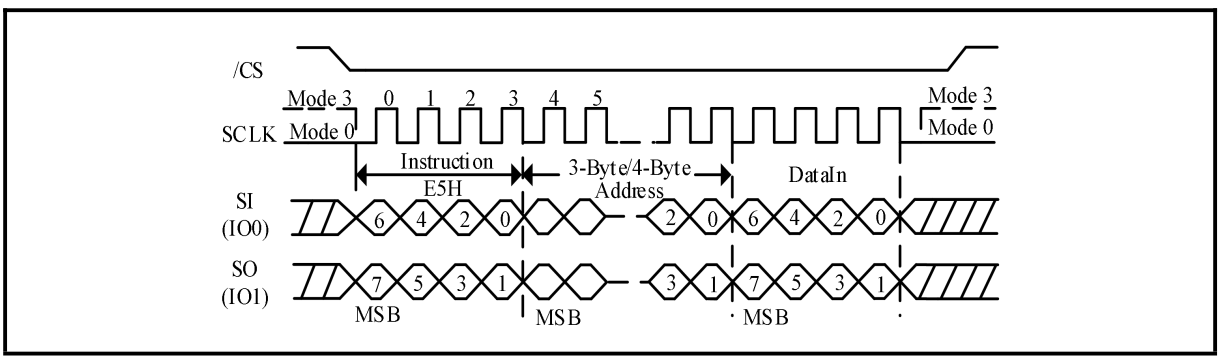
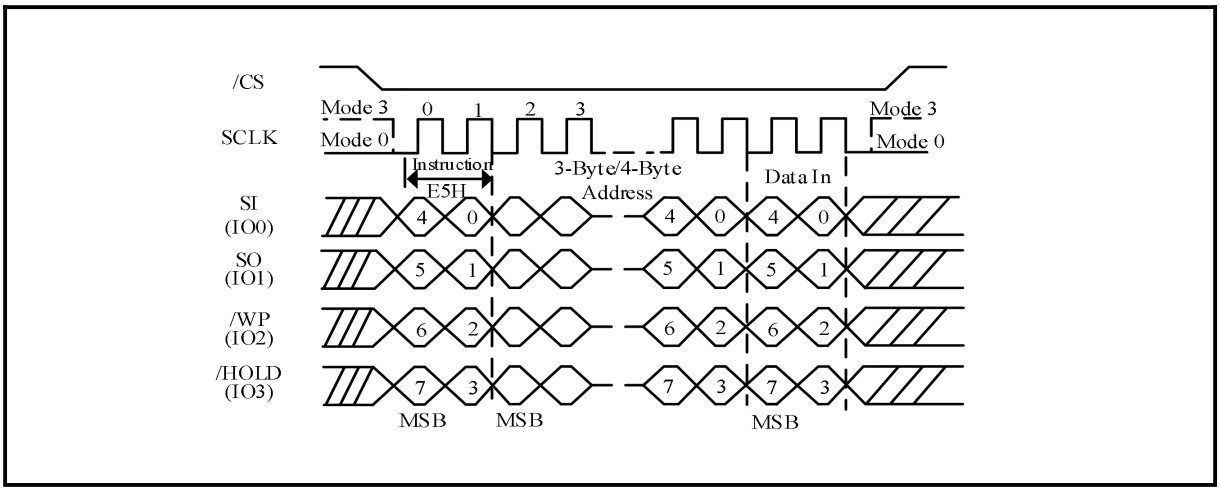


Figure 36. Write lock Register Sequence Diagram (Quad I/O Mode)



Note:

1. Write Lock Register instruction support 3-byte address and 4-byte address mode.

7.1.14 Clear Flag Status Register (50H)

See ***Figure 37-Figure 38***, to execute the Clear Flag Status Register instruction and clear the error bits (Erase, Program, and Protection), /CS is driven low. For extended SPI protocol, the instruction code is input on SI. For dual SPI protocol, the instruction code is input on IO0-IO1. For quad SPI protocol, the instruction code is input on IO0-IO3. The operation is terminated by driving /CS high at any time.

Figure 37. Clear Flag Status Register (Extended SPI Mode)

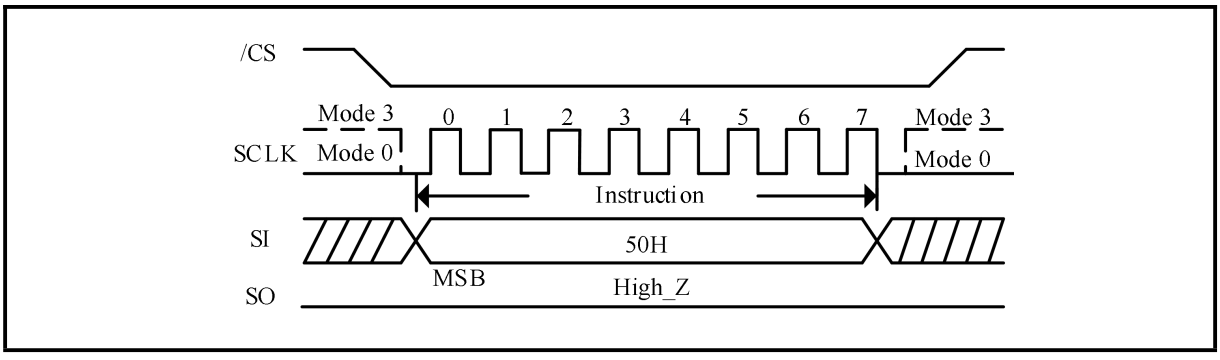
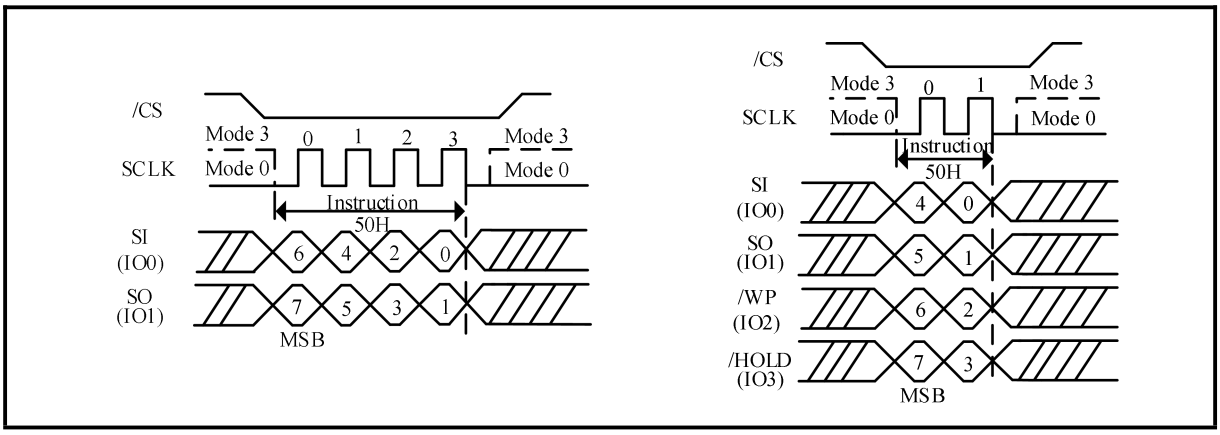


Figure 38. Clear Flag Status Register (Dual/Quad I/O Mode)



7.1.15 Enter 4-Byte Address Mode (B7H)

The Enter 4-Byte Address Mode instruction (see the ***Figure 39-Figure 40***) will allow 32-bit address (A31-A0) to be used to access the memory array beyond 128Mb. To enter or exit the 4-byte address mode, the Write Enable instruction must be executed to set the write enable latch bit to 1. The Enter 4-Byte Address Mode instruction is entered by driving /CS low. The effect of the instruction is immediate; after the instruction has been executed, the Write Enable Latch bit is cleared to 0.

Figure 39. Enter 4-Byte Address Mode instruction (Extended SPI Mode)

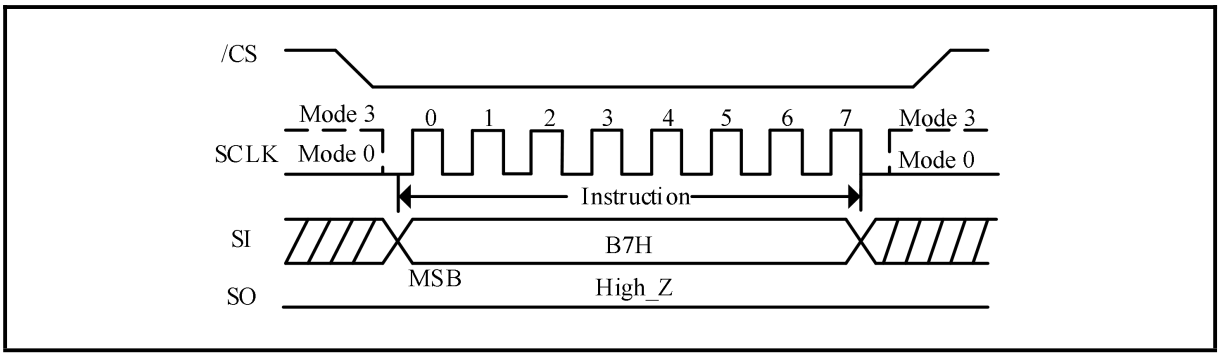
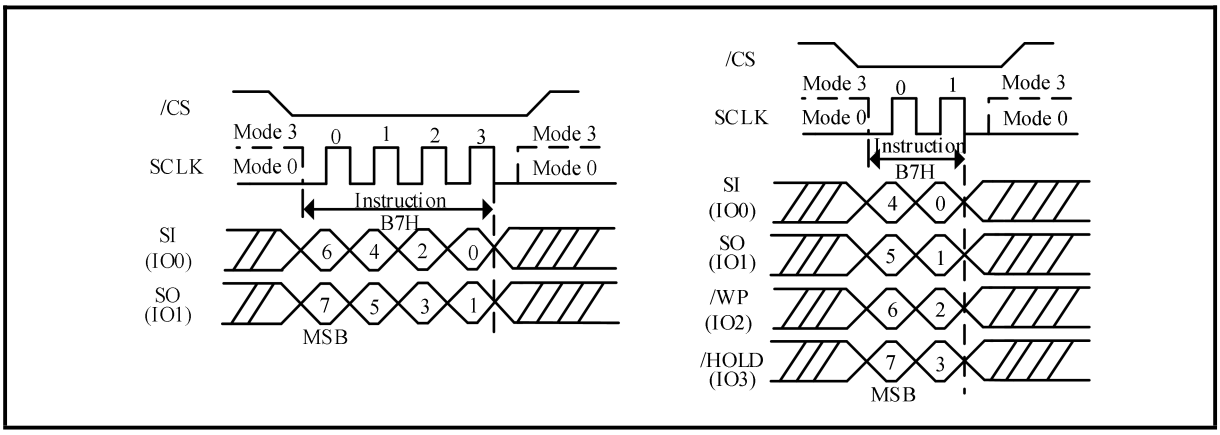


Figure 40. Enter 4-Byte Address Mode instruction (Dual I/O Mode)



7.1.16 Exit 4-Byte Address Mode (E9H)

In order to be backward compatible, the Exit 4-Byte Address Mode instruction ***(Figure 41-Figure 42***) will only allow 24-bit address (A23-A0) to be used to access the memory array up to 128Mb. The Extended Address Register must be used to access the memory array beyond 128Mb. The Exit 4-Byte Address Mode instruction is entered by driving /CS low. The effect of the instruction is immediate; after the instruction has been executed, the Write Enable Latch bit is cleared to 0.

Figure 41. Exit 4-Byte Address Mode (SPI Mode)

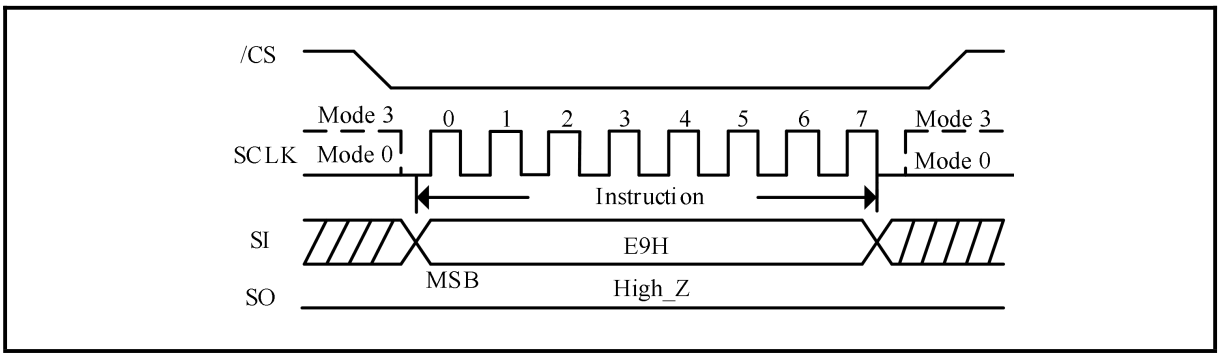
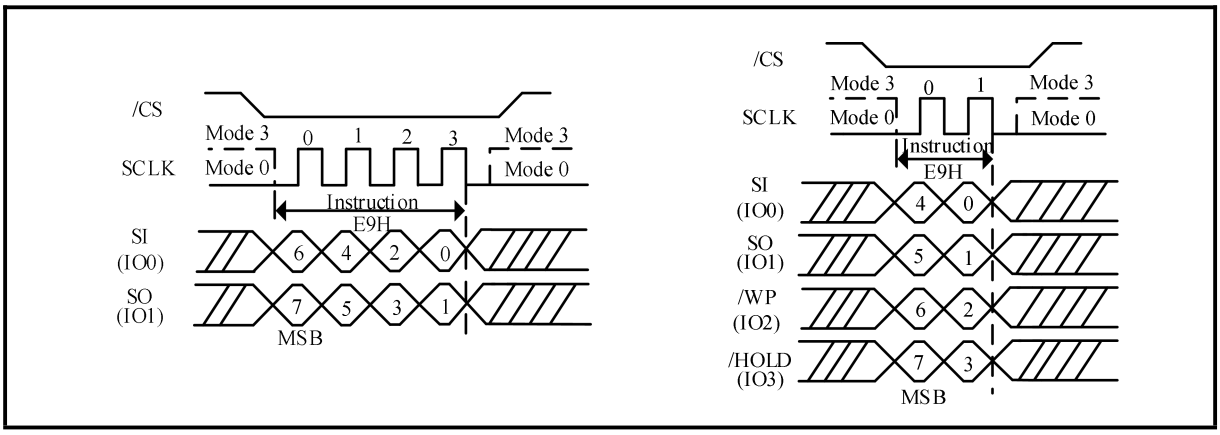


Figure 42. Exit 4-Byte Address Mode (Dual I/O Mode)



7.1.17 Reset Enable (66H) and Reset Memory (99H)

Because of the small package and the limitation on the number of pins, the memory provides a software Reset instruction instead of a dedicated Reset pin. Once the software Reset instruction is accepted, any on-going internal operations will be terminated and the device will return to its default power-on state and all volatile lock bits, the volatile configuration register, the enhanced volatile configuration register, and the extended address register are reset to the power-on reset default condition. The power-on reset condition depends on settings in the nonvolatile configuration register.

If a reset is initiated while a Write, Program, or Erase operation is in progress or suspended, the operation is aborted and data may be corrupted.

To avoid accidental reset, both “Enable Reset (66h)” and “Reset (99h)” instructions must be issued in sequence. Any other instructions other than “Reset (99h)” after the “Enable Reset (66h)” instruction will disable the “Reset Enable” state.

To execute each instruction, /CS is driven low. The instruction code is input on SI. A minimum de-selection time of tSHSL2 must come between the Reset Enable and Reset Memory instructions or a reset is not guaranteed. When these two instructions are executed and /CS is driven high, the device enters a power-on reset condition. A time of tSHSL3 is required before the device can be re-selected by driving /CS low.

The Enable Reset (66h) and Reset (99h) instruction sequence is shown in ***Figure 43-Figure 45***.

Reset is effective once bit 7 of the flag status register outputs 1 with at least one byte output. A Reset Enable instruction is not accepted in the cases of Write Status Register and Write Nonvolatile Configuration Register operations.

Figure 43. Reset Enable (66h) and Reset Memory (99h) Instruction (Extended SPI Mode)

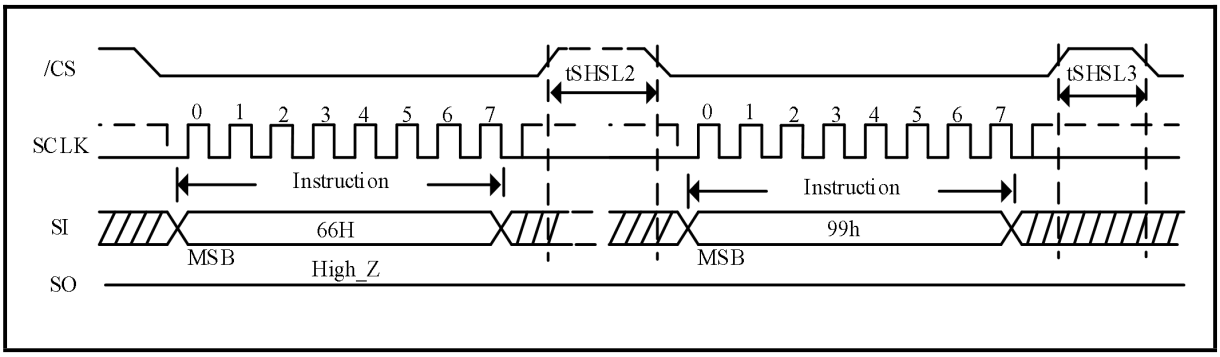


Figure 44. Reset Enable (66h) and Reset Memory (99h) Instruction (Dual I/O Mode)

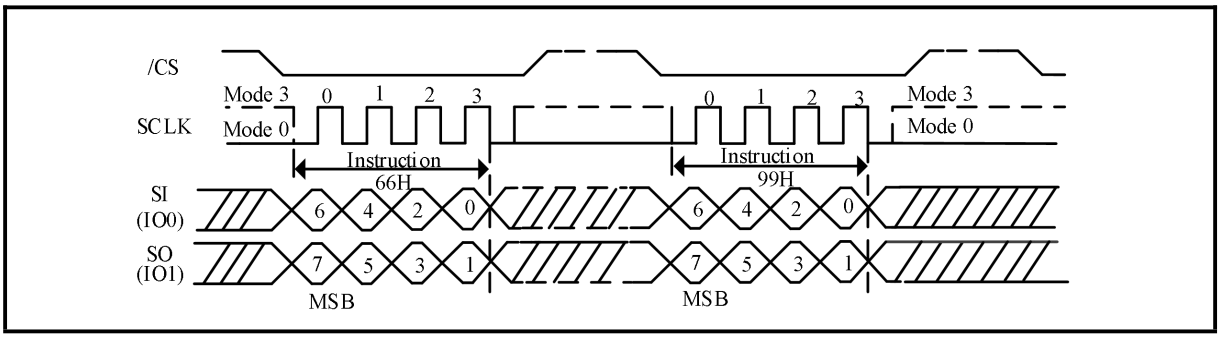
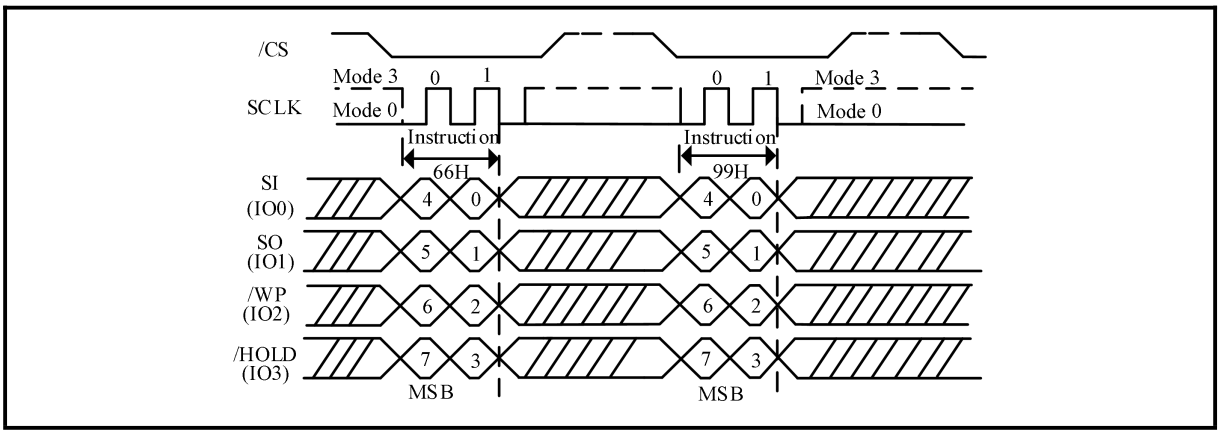


Figure 45. Reset Enable (66h) and Reset (99h) Memory Instruction (Quad I/O Mode)



Note:

1. The number of lines and rate for transmission varies with extended, dual, or quad SPI.

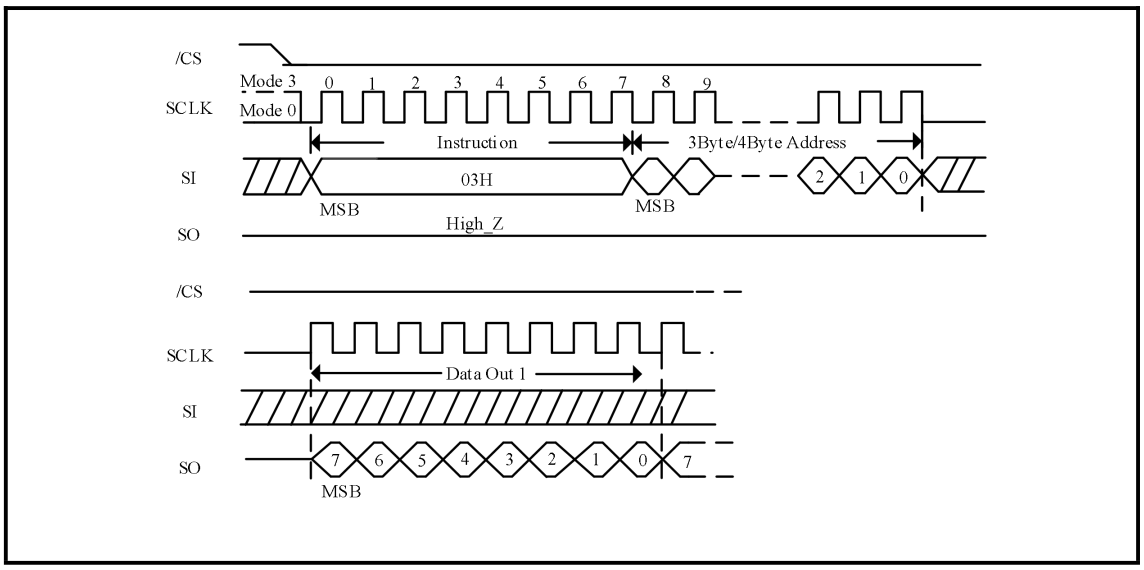
7.2 Read Memory Instructions

7.2.1 Read Data (03H)

See ***Figure 46***, the Read Data instruction is followed by a 3-byte/4-byte address (A23/31-A0), each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, during the falling edge of SCLK. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. This means that the entire memory can be accessed with a single instruction as long as the clock continues. The instruction is completed by driving /CS high. The whole memory can be Read with a single Read Data instruction. Any Read Data instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress. The instruction only Support Extended SPI protocol.

After Read Data instruction is executed, the device will output data from the selected address in the die. After a die boundary is reached, the device will start Reading again from the beginning of the same 256Mb die. A complete device Reading is completed by executing Read four times.

Figure 46. Read Instruction Sequence Diagram (Extended SPI Mode)



7.2.2 Fast Read (0BH)

See ***Figure 47-Figure 49***, the Read Data Bytes at Higher Speed (Fast Read) instruction is for quickly Reading data out. It is followed by a 3-byte/4-byte address (A23/31-A0) and a dummy byte, each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO (for dual I/O protocol is IO0-IO1, quad I/O protocol is IO0-IO3), each bit being shifted out, at a Max frequency Fc, during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

After Read instruction is executed, the device will output data from the selected address in the die. After a die boundary is reached, the device will start Reading again from the beginning of the same 256Mb die. A complete device Reading is completed by executing Read four times.

Figure 47. Fast Read Instruction Sequence Diagram (Extended SPI Mode)

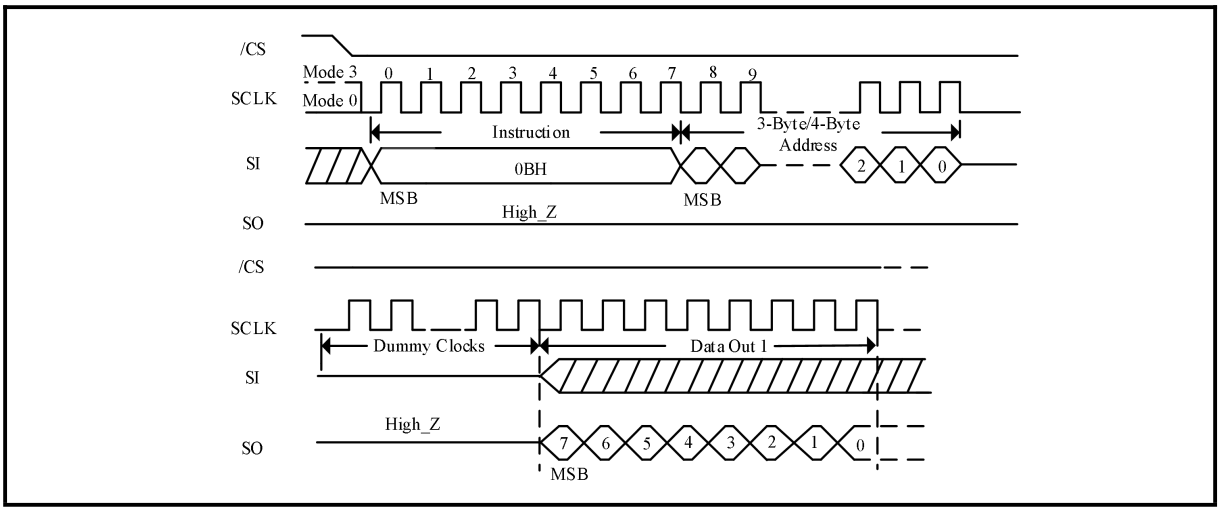


Figure 48. Fast Read Instruction Sequence Diagram (Dual I/O Mode)

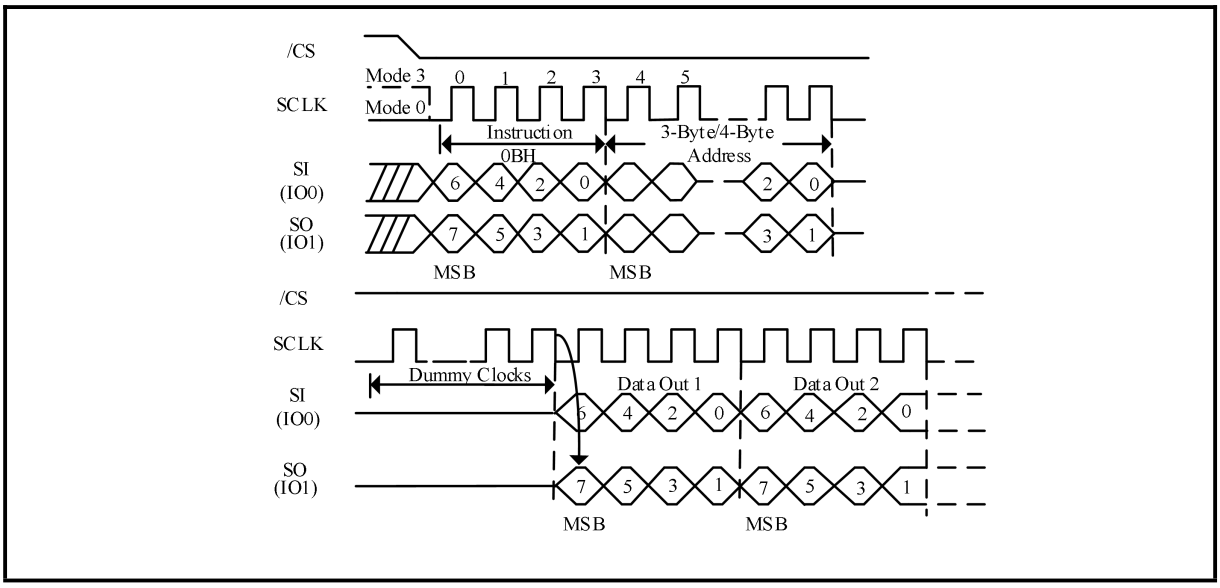
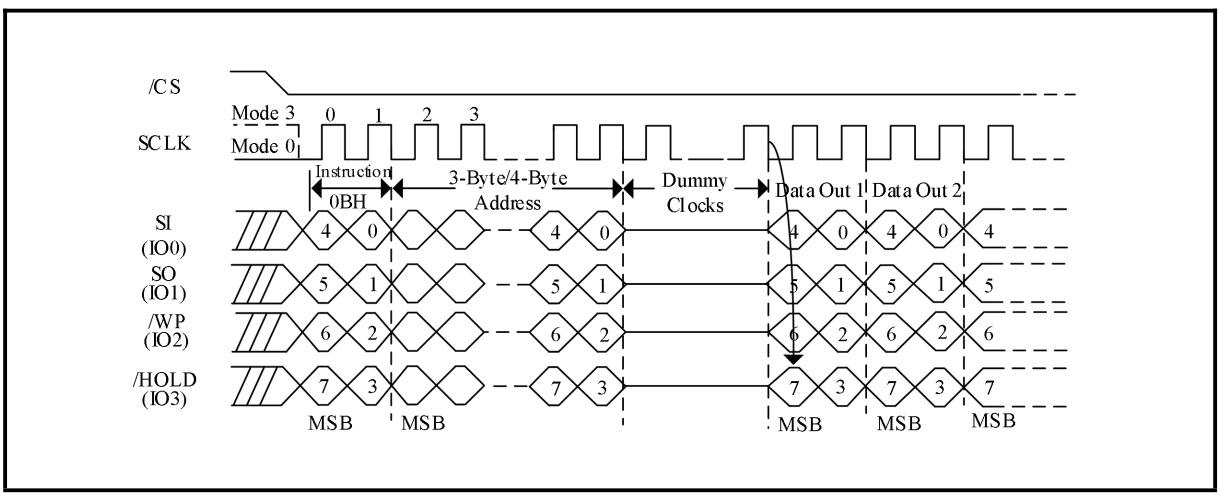


Figure 49. Fast Read Instruction Sequence Diagram (Quad I/O Mode)



Note:

1. Fast Read instruction support 3-byte address and 4-byte address mode.
2. Dummy clock cycles can be set by the user through the Nonvolatile and Volatile Configuration Registers (See the ***Table 9*** and ***Table 10***).

7.2.3 Dual Output Fast Read (3BH)

See ***Figure 50-Figure 51***, the Dual Output Fast Read instruction is followed by 3/4-byte address (A23/31-A0) and a dummy byte, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from IO0 and IO1. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The instruction support Extended SPI and Dual I/O SPI protocol.

After Read instruction is executed, the device will output data from the selected address in the die. After a die boundary is reached, the device will start Reading again from the beginning of the same 256Mb die. A complete device Reading is completed by executing Read four times.

Figure 50. Dual Output Fast Read Sequence Diagram (Extended SPI Mode)

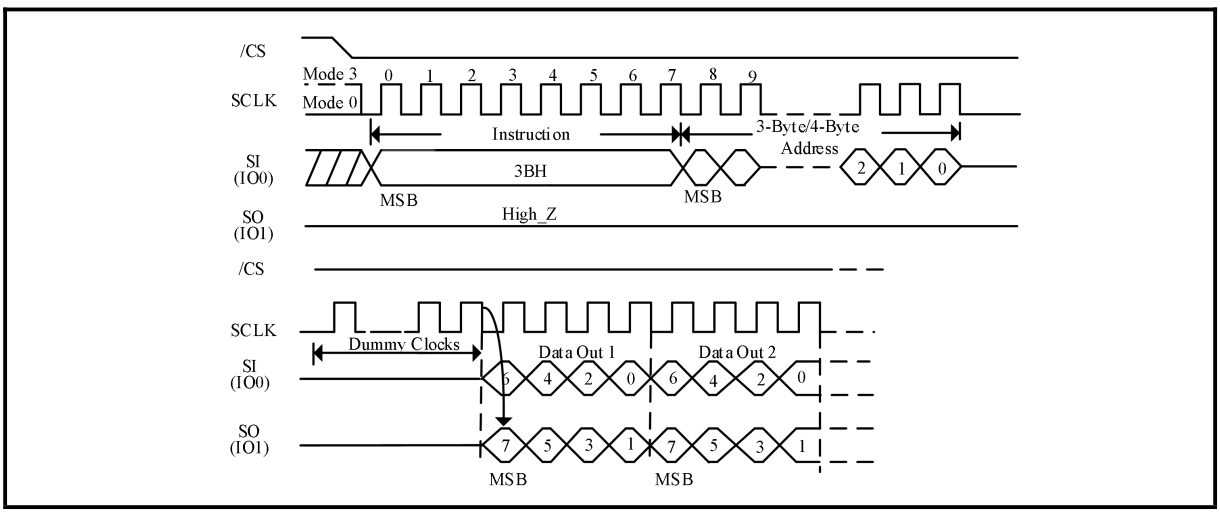
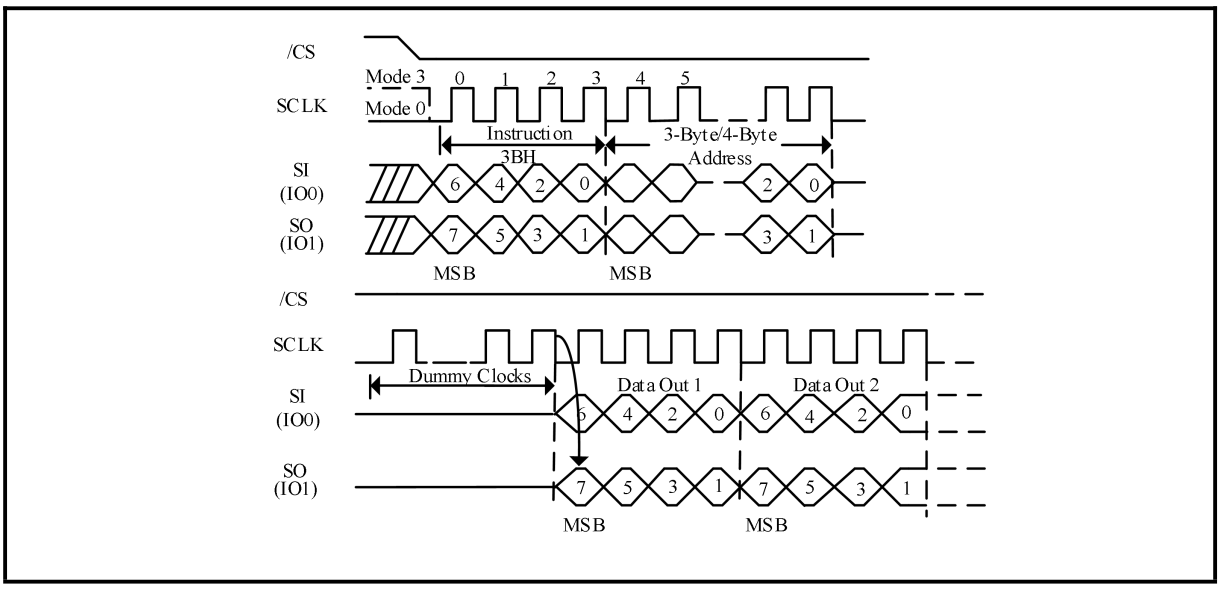


Figure 51. Dual Output Fast Read Sequence Diagram (Dual I/O Mode)



Note:

1. Dual Output Fast Read instruction support 3-byte address and 4-byte address mode.
2. Dummy clock cycles can be set by the user through the Nonvolatile and Volatile Configuration Registers (See the ***Table 9*** and ***Table 10***).

7.2.4 Dual Input/Output Fast Read (BBH)

See ***Figure 52-Figure 53***, the Dual Input/Output Fast Read instruction is similar to the Dual Output Fast Read instruction except that it requires address transfer in IO0 and IO1 for Extended SPI protocol. The Dual Input/Output Fast Read instruction is followed by 3/4-byte address (A23/31-A0) and a dummy byte, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from IO0 and IO1. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The instruction support Extended SPI and Dual I/O SPI protocol.

After Read instruction is executed, the device will output data from the selected address in the die. After a die boundary is reached, the device will start Reading again from the beginning of the same 256Mb die. A complete device Reading is completed by executing Read four times.

Figure 52. Dual Input/Output Fast Read (Extended SPI Mode)

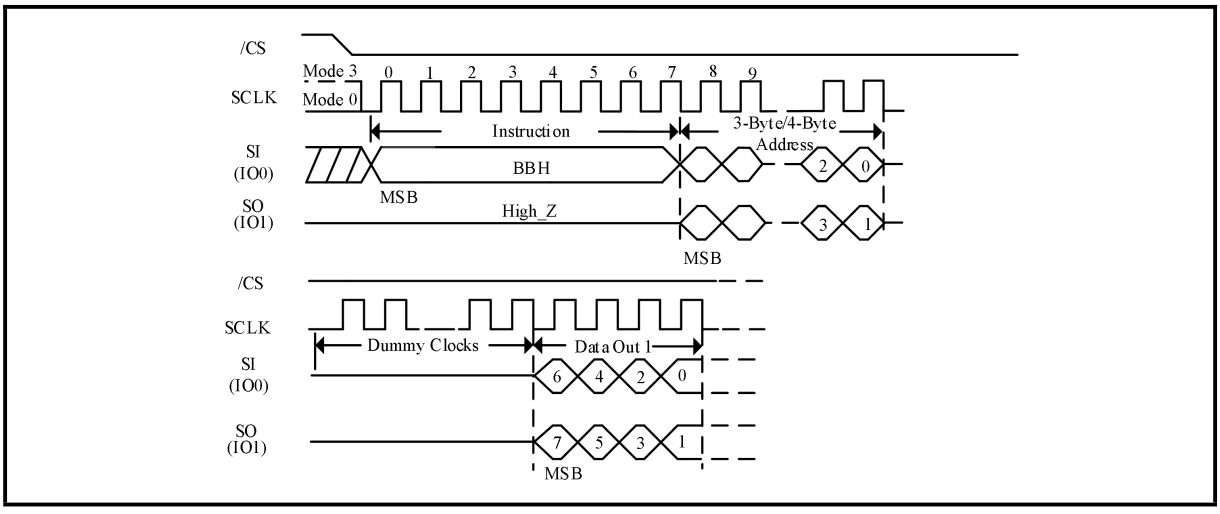
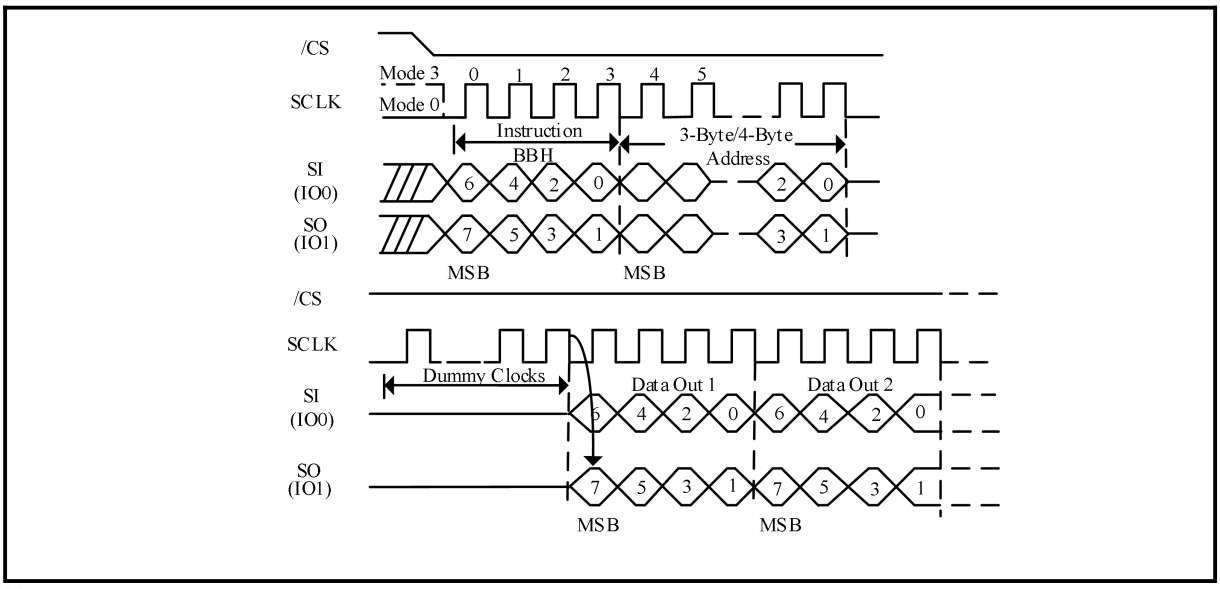


Figure 53. Dual Input/Output Fast Read (Dual I/O Mode)



Note:

1. The Dual Input/Output Fast Read instruction support 3-byte address and 4-byte address mode.
2. Dummy clock cycles can be set by the user through the Nonvolatile and Volatile Configuration Registers (See the ***Table 9*** and ***Table 10***).

7.2.5 Quad Output Fast Read (6BH)

See ***Figure 54-Figure 55***, the Quad Output Fast Read instruction is followed by 3/4-byte address (A23/31-A0) and a dummy byte, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 4-bit per clock cycle from IO0, IO1, IO2 and IO3. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The instruction support Extended SPI and Quad I/O SPI protocol.

After Read instruction is executed, the device will output data from the selected address in the die. After a die boundary is reached, the device will start Reading again from the beginning of the same 256Mb die. A complete device Reading is completed by executing Read four times.

Figure 54. Quad Output Fast Read (Extended SPI Mode)

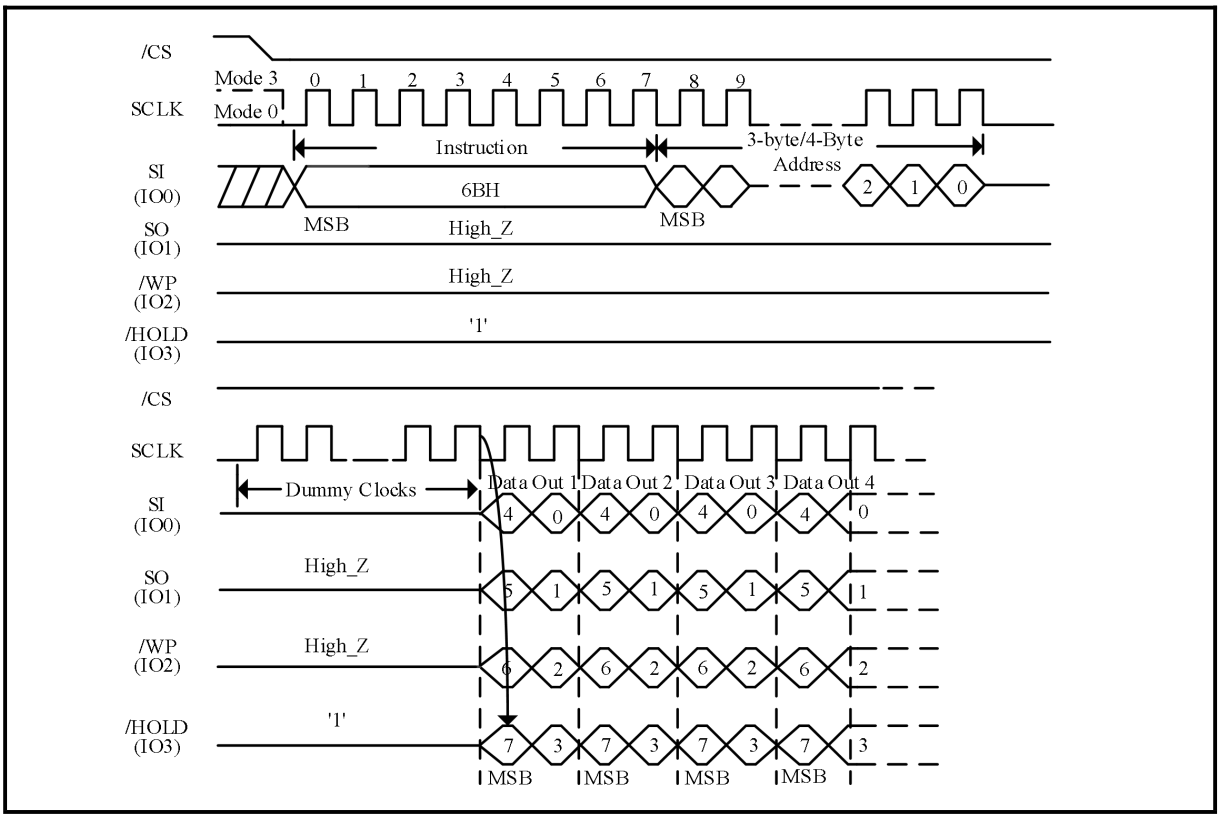
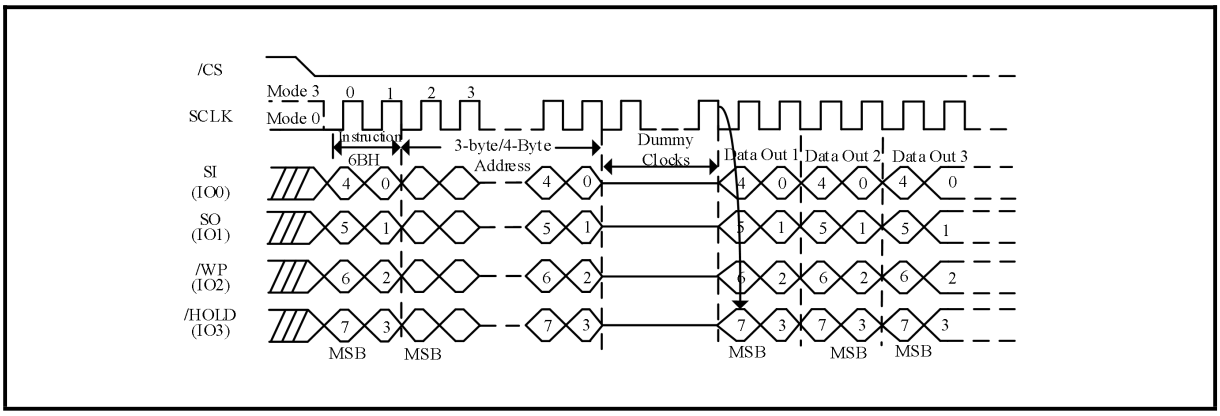


Figure 55. Quad Output Fast Read (Quad I/O Mode)



Note:

1. The Quad Output Fast Read instruction support 3-byte address and 4-byte address mode.
2. Dummy clock cycles can be set by the user through the Nonvolatile and Volatile Configuration Registers (See the ***Table 9*** and ***Table 10***).

7.2.6 Quad Input/Output Fast Read (EBH)

See ***Figure 56-Figure 57***, the Quad Input/Output Fast Read instruction is similar to the Quad Output Fast Read instruction except that it requires address transfer in IO0, IO1, IO2 and IO3 for Extended SPI protocol. The Quad Input/Output Fast Read instruction is followed by 3/4-byte address (A23/31-A0) and a dummy byte, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 4-bit per clock cycle from IO0, IO1, IO2 and IO3. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The instruction support Extended SPI and Quad I/O SPI protocol.

After Read instruction is executed, the device will output data from the selected address in the die. After a die boundary is reached, the device will start Reading again from the beginning of the same 256Mb die. A complete device Reading is completed by executing Read four times.

Figure 56. Quad Input/Output Fast Read (Extended SPI Mode)

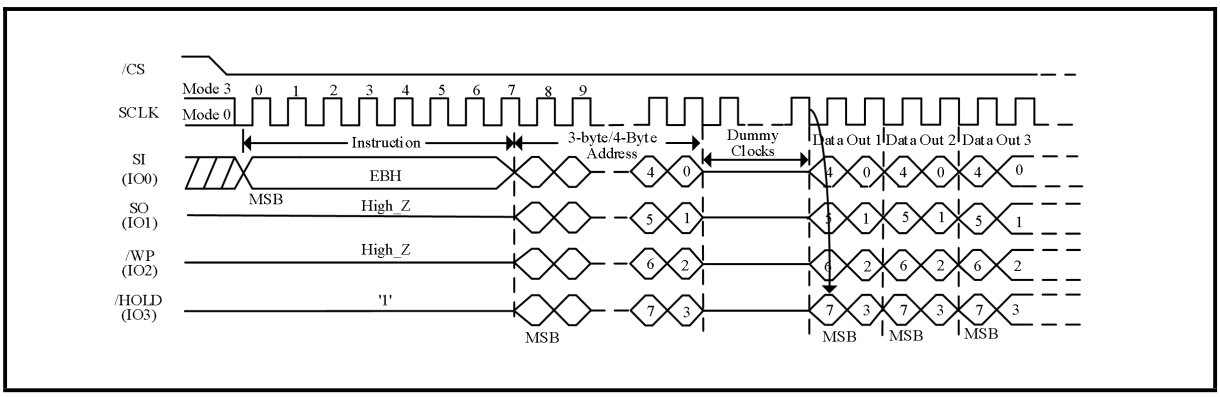
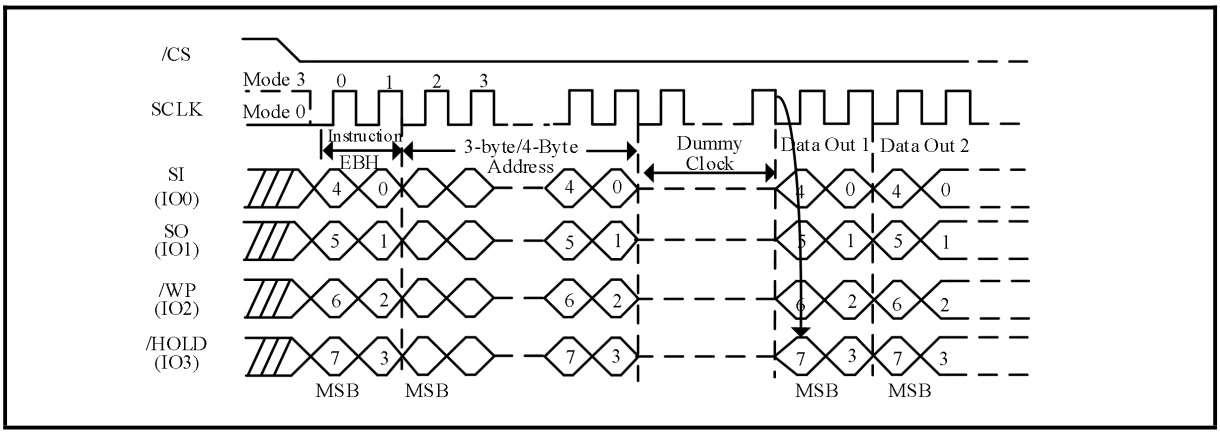


Figure 57. Quad Input/Output Fast Read (Quad I/O Mode)



Note:

1. The Quad Input/Output Fast Read instruction support 3-byte address and 4-byte address mode.
2. Dummy clock cycles can be set by the user through the Nonvolatile and Volatile Configuration Registers (See the ***Table 9*** and ***Table 10***).

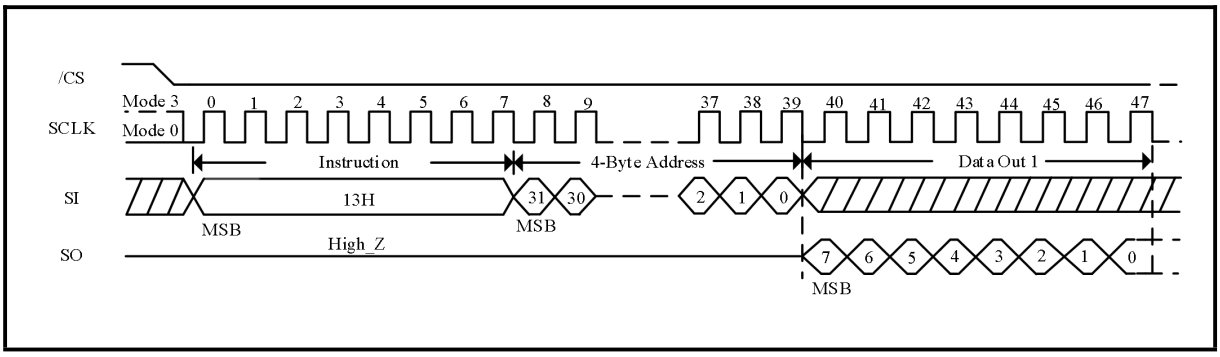
7.2.7 4-Byte Read (13H)

The 4-Byte Read instruction is similar to the Read Data (03H) instruction. Instead of 24-bit address, 32-bit address is needed following the instruction code 03/13H. No matter the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the Read Data with 4-Byte Address instruction will always require 32-bit address to access the entire 1Gb memory.

The 4-Byte Read instruction sequence is shown in ***Figure 58***. The 4-Byte Read instruction allows clock rates from D.C. to a maximum of fR (see AC Electrical Characteristics).

The Read Data with 4-Byte Read (13H) instruction is only supported in Extended SPI mode.

Figure 58. 4-Byte Read Sequence Diagram (Extended SPI Mode)



7.2.8 4-Byte Fast Read (0CH)

See ***Figure 59-Figure 61***, the 4-Byte Fast Read (0CH) instruction is similar to the Fast Read instruction except that it requires 32-bit address instead of 24-bit address. No matter the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the Read Data with 4-Byte Address instruction will always require 32-bit address to access the entire 1Gb memory.

The 4-Byte Fast Read (0CH) instruction is supported in Extended SPI, Dual I/O and Quad I/O SPI mode.

Figure 59. 4-Byte Fast Read Sequence Diagram (Extended SPI Mode)

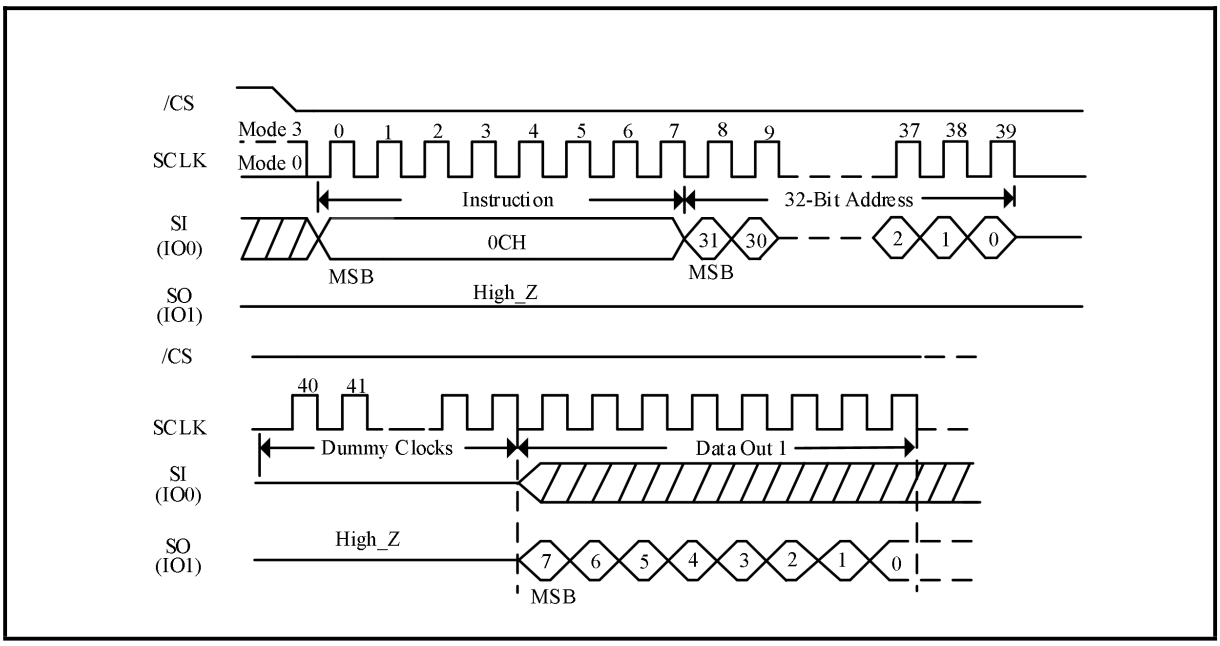


Figure 60. 4-Byte Fast Read Sequence Diagram (Dual I/O Mode)

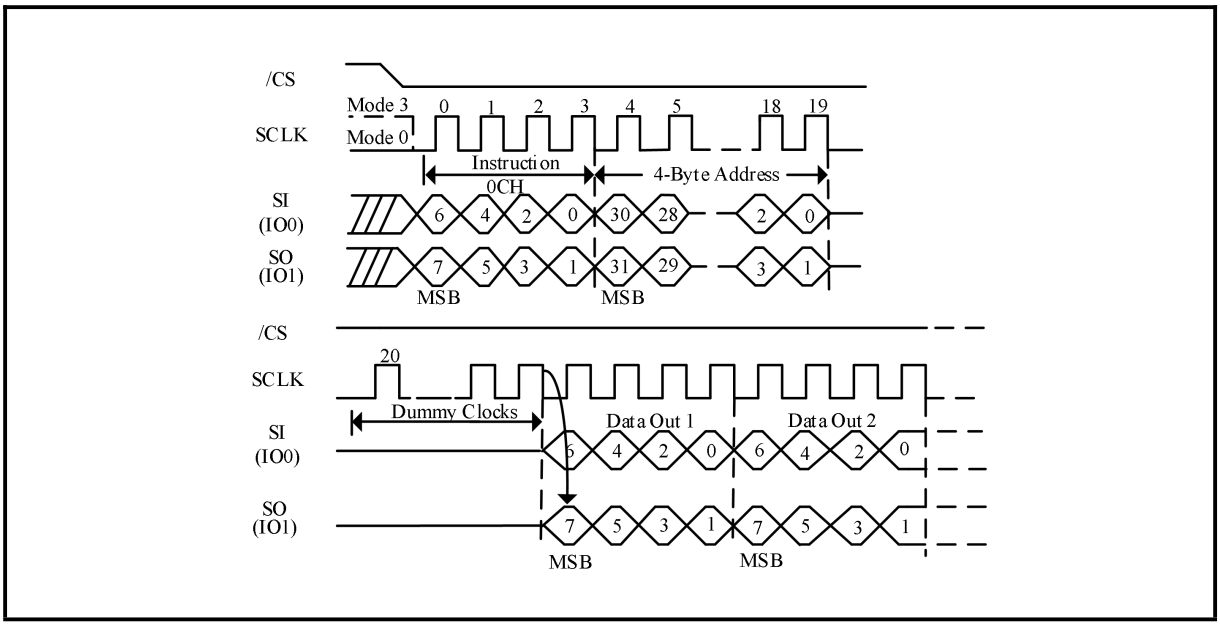
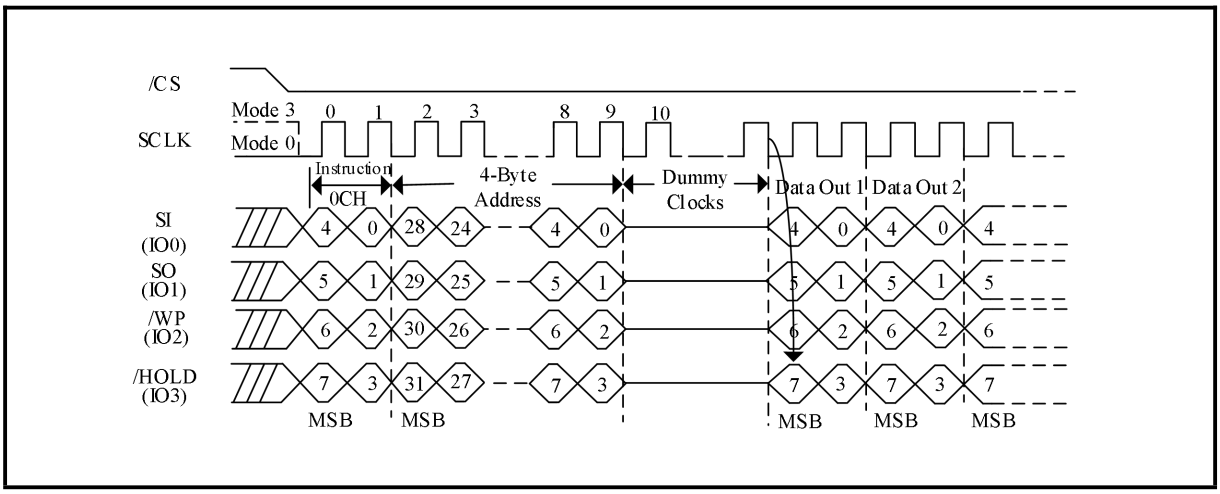


Figure 61. 4-Byte Fast Read Sequence Diagram (Quad I/O Mode)



Note:

1. Dummy clock cycles can be set by the user through the Nonvolatile and Volatile Configuration Registers (See the ***Table 9*** and ***Table 10***).

7.2.9 4-Byte Dual Output Fast Read (3CH)

See ***Figure 62-Figure 63***, the 4-Byte Dual Output instruction is similar to the Dual Output Fast Read instruction except that it requires 32-bit address instead of 24-bit address. No matter the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the 4-Byte Dual Output Fast Read instruction will always require 32-bit address to access the entire 1Gb memory.

The 4-Byte Dual Output (3CH) instruction is supported in Extended SPI and Dual I/O SPI mode.

Figure 62. 4-Byte Dual Output Fast Read Sequence Diagram (Extended SPI Mode)

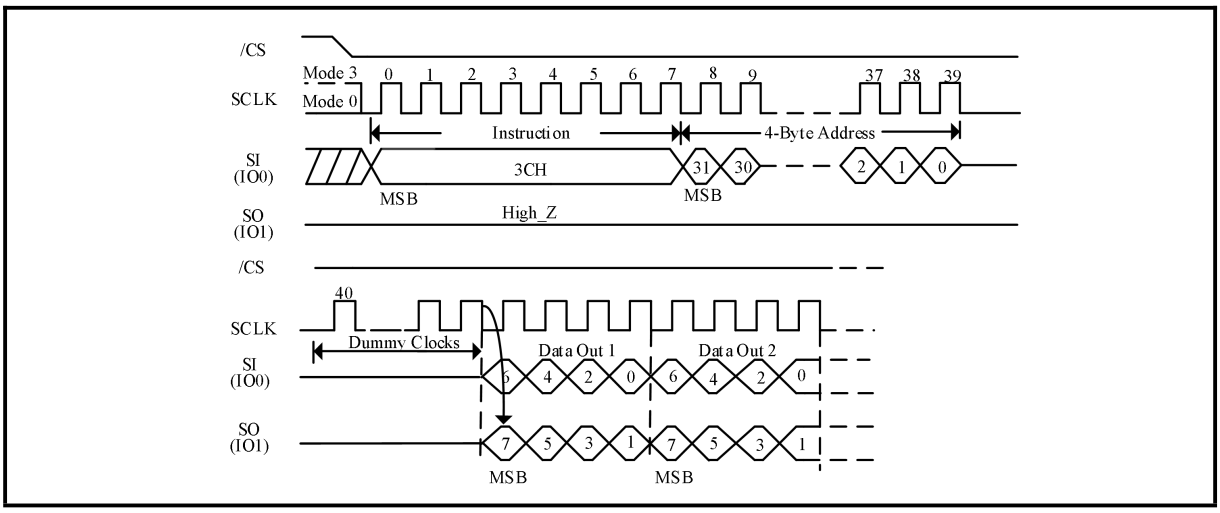
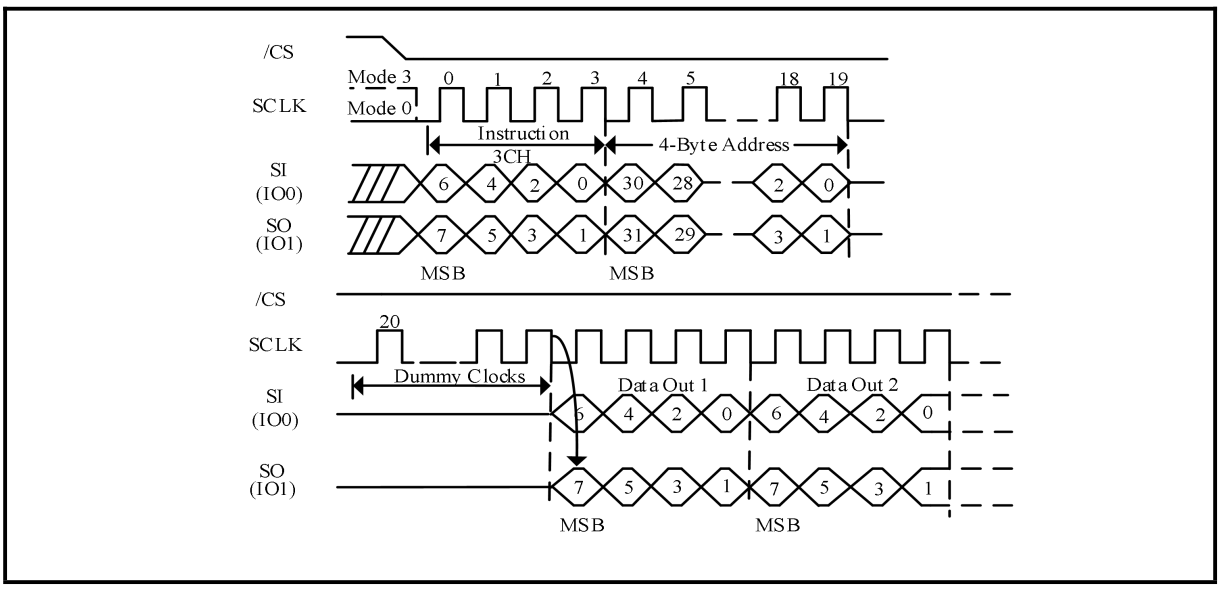


Figure 63. 4-Byte Dual Output Fast Read Sequence Diagram (Dual I/O Mode)



Note:

1. Dummy clock cycles can be set by the user through the Nonvolatile and Volatile Configuration Registers (See the ***Table 9*** and ***Table 10***).

7.2.10 4-Byte Dual Input/Output Fast Read (BCH)

See ***Figure 64-Figure 65***, the 4-Byte Dual Input/Output instruction is similar to the 4-Byte Dual Output Fast Read instruction except that it requires 32-bit address transfer in IO0 and IO1 for Extended SPI protocol. No matter the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the Fast Read Dual Output with 4-Byte Address instruction will always require 32-bit address to access the entire 256Mb memory.

The 4-Byte Dual Input/Output (BCH) instruction is supported in Extended SPI and Dual I/O SPI mode.

Figure 64. 4-Byte Dual Input/Output Fast Read (Extended SPI Mode)

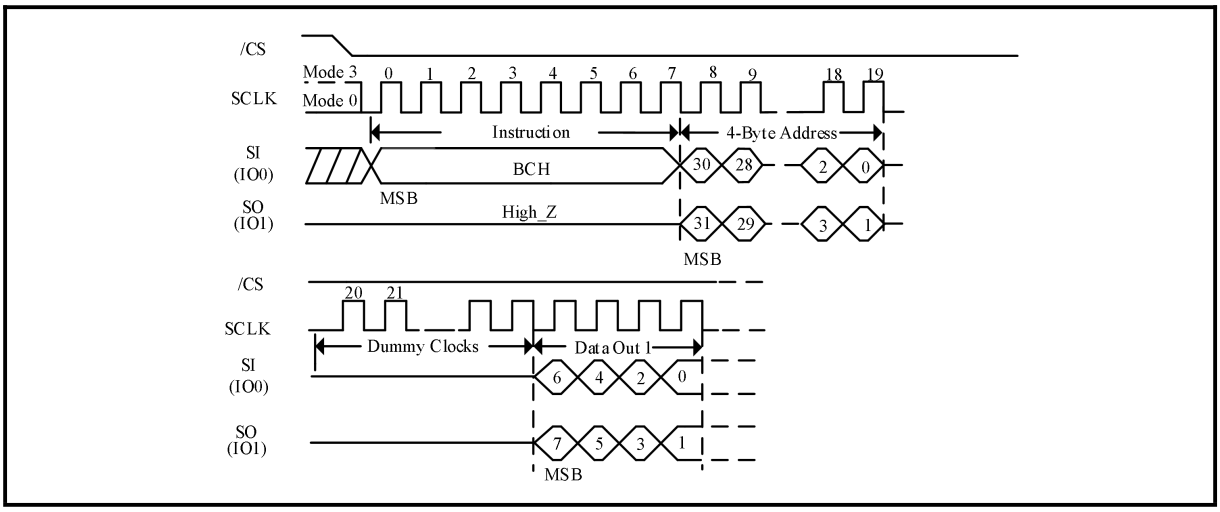
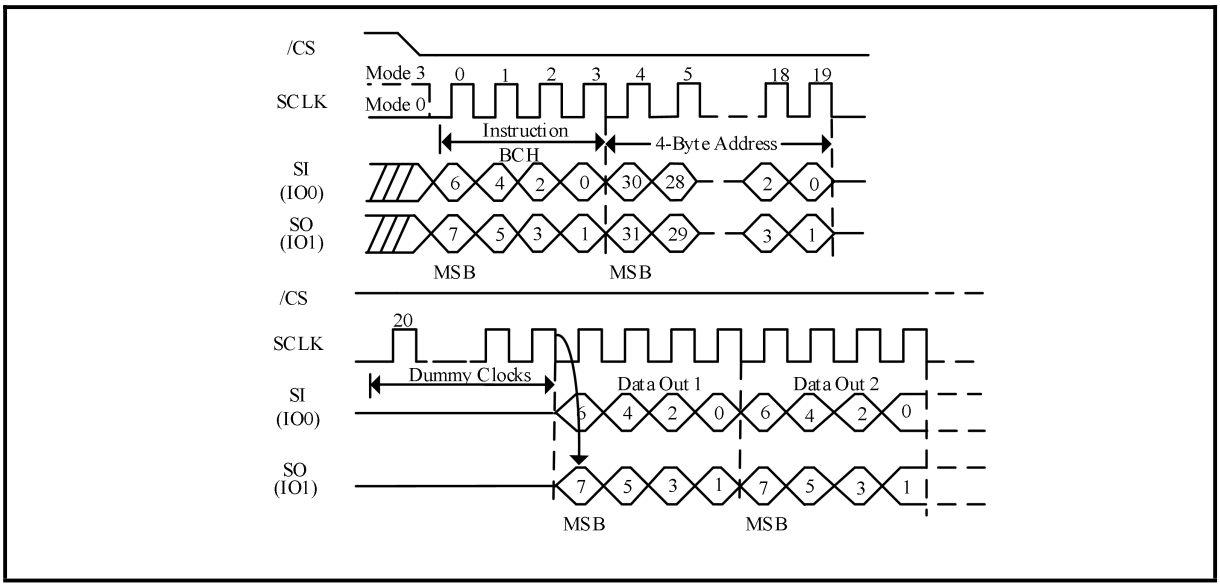


Figure 65. 4-Byte Dual Input/Output Fast Read (Dual I/O Mode)



Note:

1. Dummy clock cycles can be set by the user through the Nonvolatile and Volatile Configuration Registers (See the ***Table 9*** and ***Table 10***).

7.2.11 4-Byte Quad Output Fast Read (6CH)

See ***Figure 66-Figure 67***, The 4-Byte Quad Output instruction is similar to the Quad Output Fast Read instruction except that it requires 32-bit address instead of 24-bit address. No matter the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the 4-Byte Quad Output Fast Read instruction will always require 32-bit address to access the entire 1Gb memory.

The 4-Byte Quad Output (6CH) instruction is supported in Extended SPI and Quad I/O SPI mode.

Figure 66. 4-Byte Quad Output Fast Read (Extended SPI Mode)

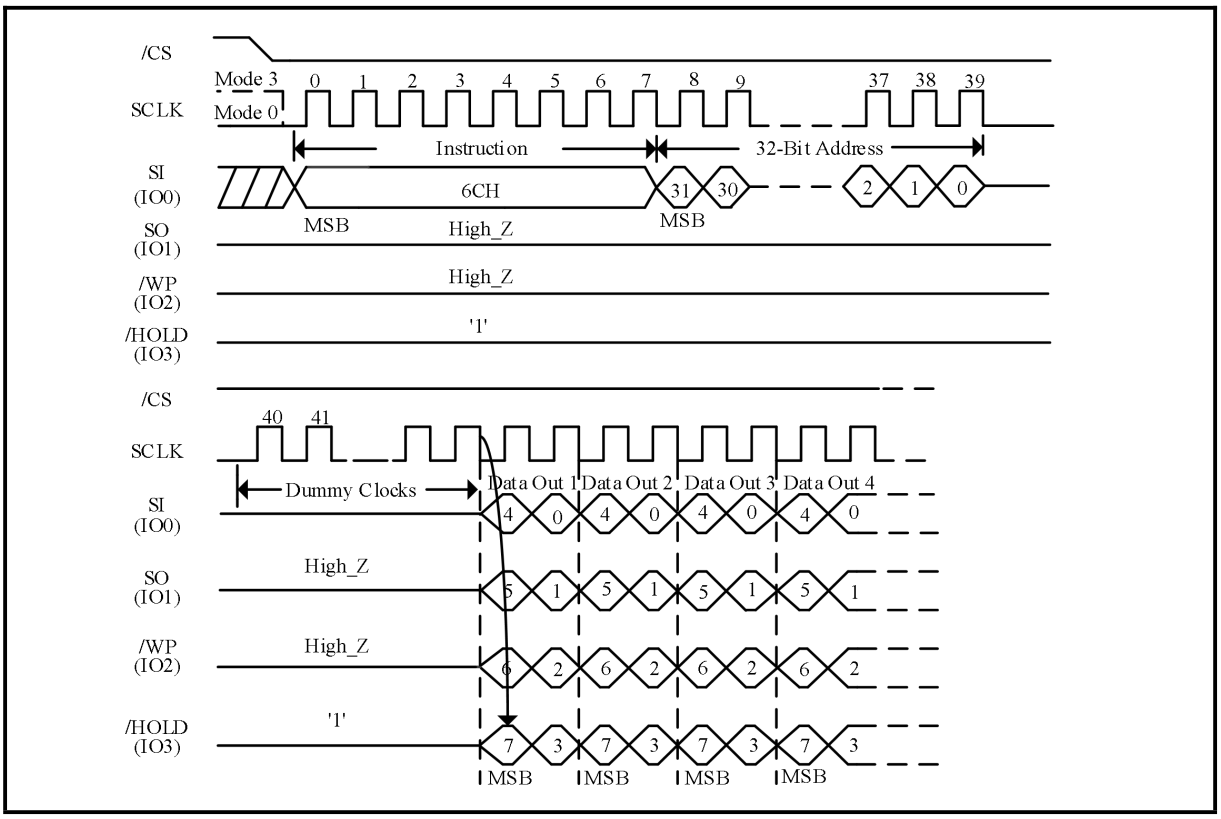
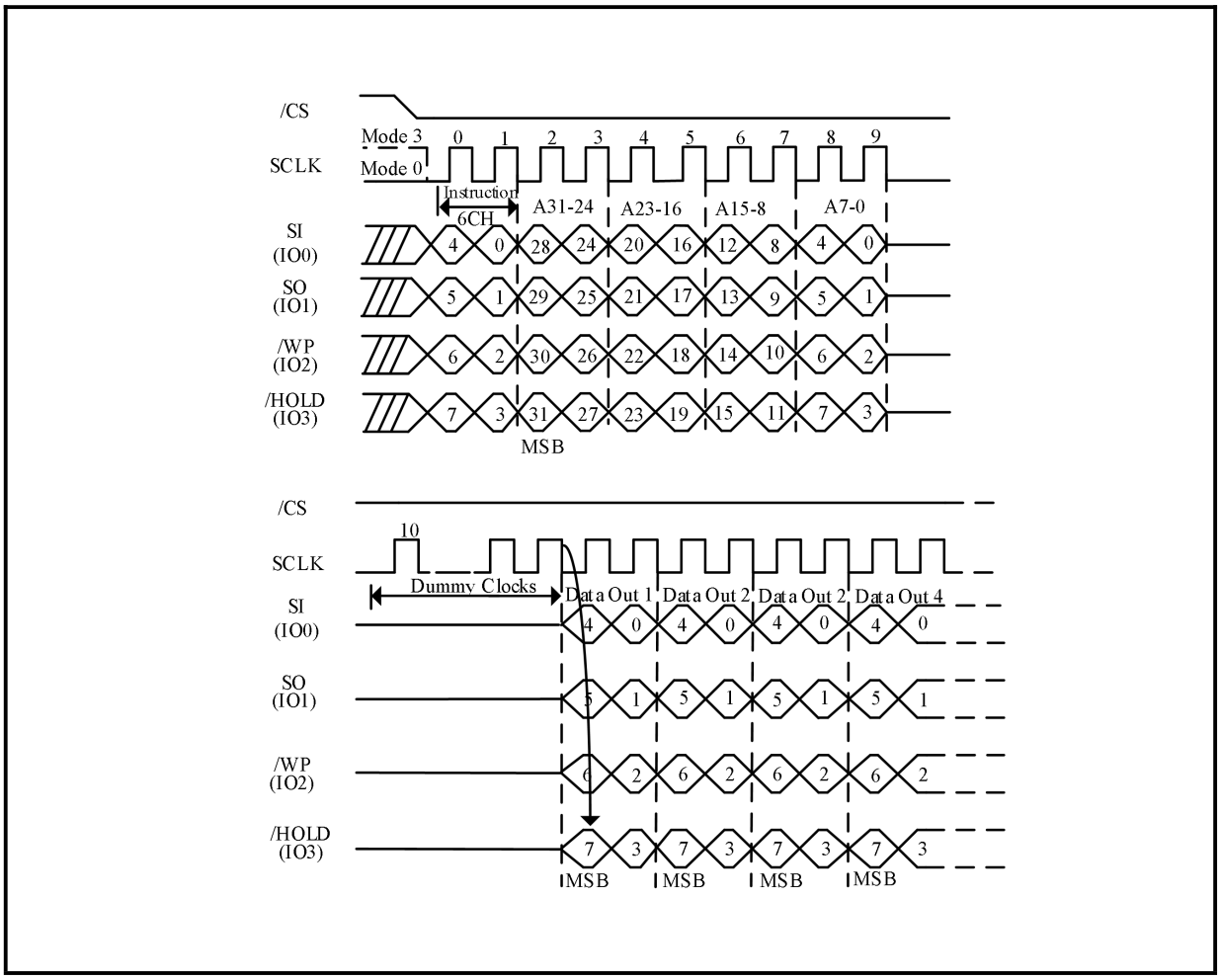


Figure 67. 4-Byte Quad Output Fast Read (Quad I/O Mode)



Note:

1. Dummy clock cycles can be set by the user through the Nonvolatile and Volatile Configuration Registers (See the ***Table 9*** and ***Table 10***).

7.2.12 4-Byte Quad Input/Output Fast Read (ECH)

The 4-Byte Quad Input/Output instruction is similar to the 4-Byte Quad Output Fast Read instruction except that it requires 32-bit address transfer in IO0, IO1, IO2 and IO3 for Extended SPI protocol. No matter the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the 4-Byte Quad Input/Output Fast Read instruction will always require 32-bit address to access the entire 256Mb memory.

The 4-Byte Quad Output (6CH) instruction is supported in Extended SPI and Quad I/O SPI mode.

Figure 68. 4-Byte Quad Input/Output Fast Read (Extended SPI Mode)

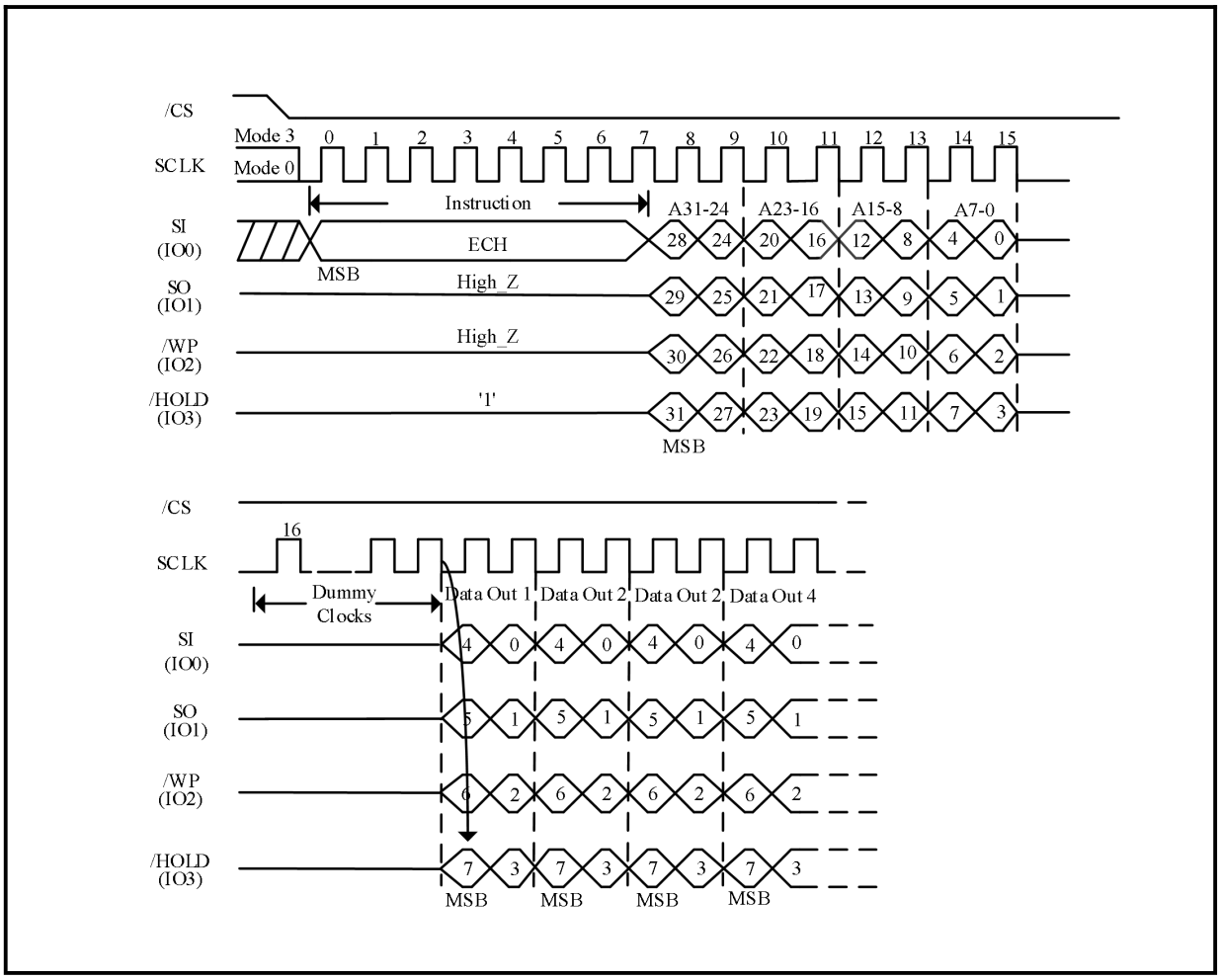
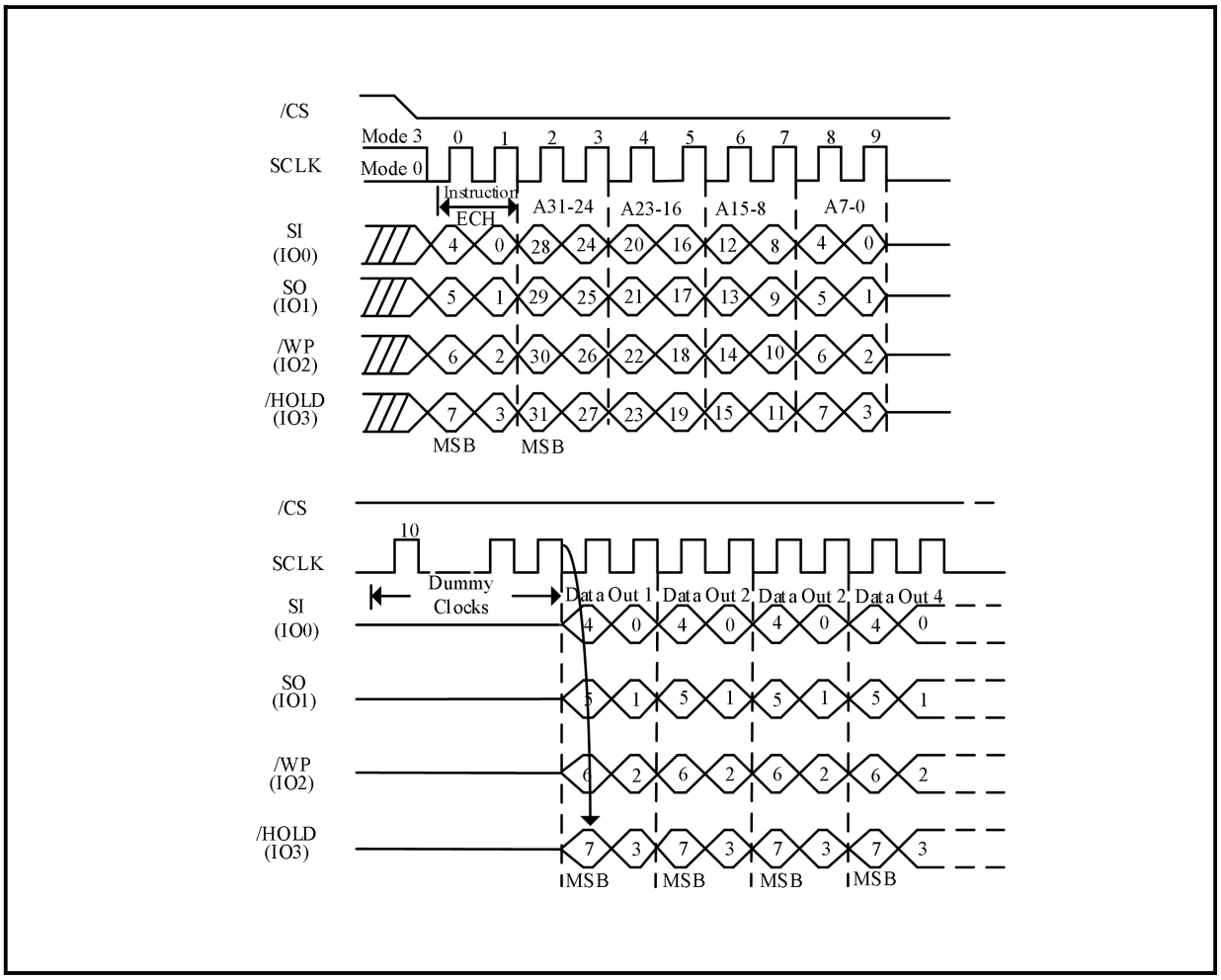


Figure 69. 4-Byte Quad Input/Output Fast Read (Quad I/O Mode)



Note:

1. Dummy clock cycles can be set by the user through the Nonvolatile and Volatile Configuration Registers (See the ***Table 9*** and ***Table 10***).

7.2.13 Fast Read-DTR (0DH)

The DTR Fast Read instruction is similar to the Fast Read instruction except that the 24/32-bit address input and the data output requires DTR (Double Transfer Rate) operation. This is accomplished by adding “dummy” clocks after the 24/32-bit address as shown in ***Figure 70-Figure 70***. The dummy clocks allow the devices internal circuits additional time for setting up the initial address. After the dummy clocks the data value on the SI pin is a "Don’t Care".

The Fast Read-DTR (0DH) instruction is supported in Extended SPI, Dual I/O SPI and Quad I/O SPI mode.

Figure 70. Fast Read-DTR Sequence Diagram (Extended SPI Mode)

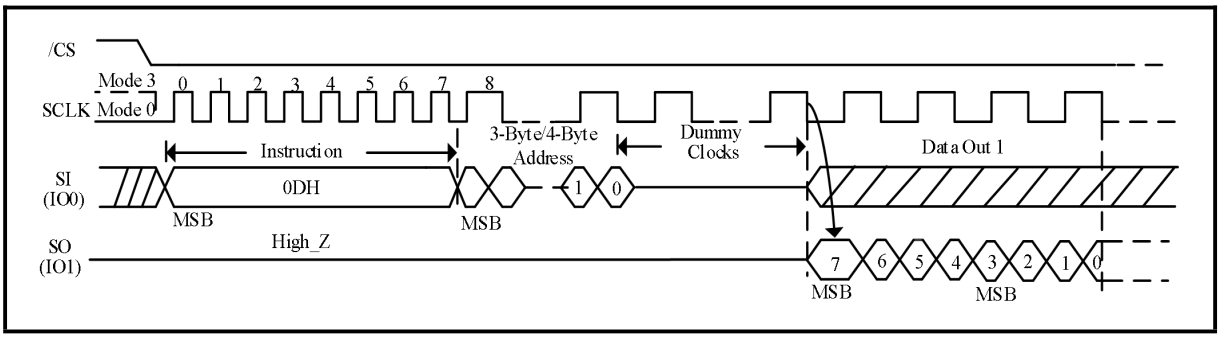


Figure 71. Fast Read-DTR Sequence Diagram (Dual I/O Mode)

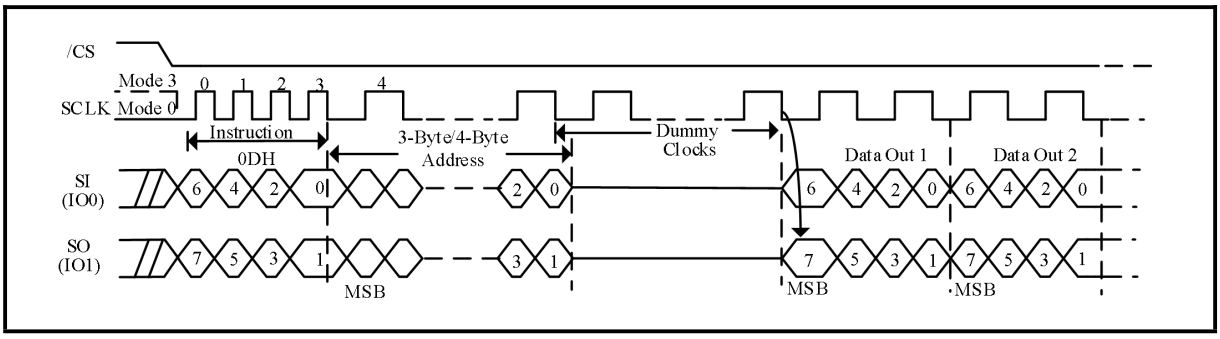
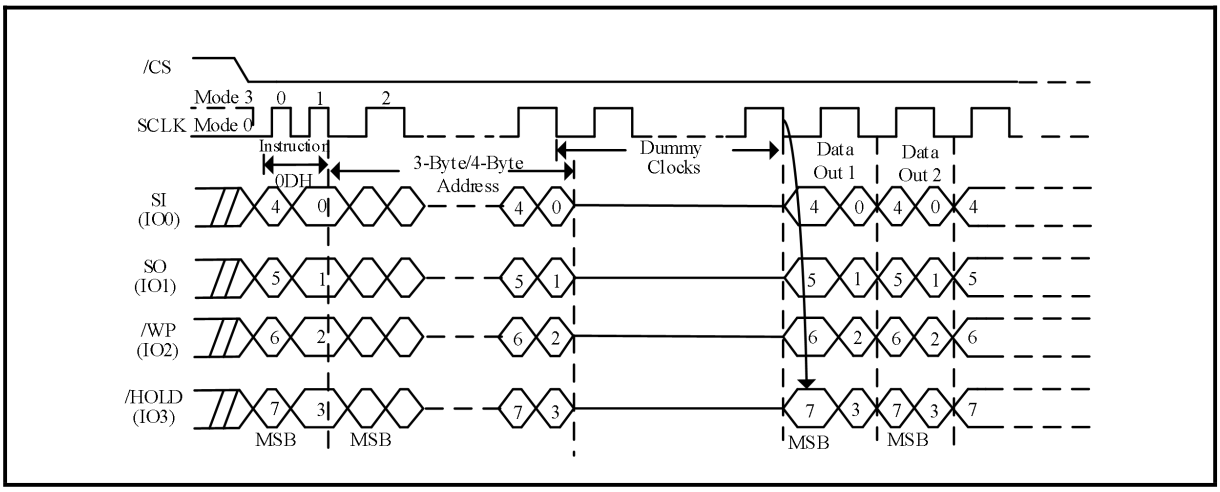


Figure 72. Fast Read-DTR Sequence Diagram (Quad I/O Mode)



Note:

1. The Fast Read-DTR instruction support 3-byte address and 4-byte address mode.
2. Dummy clock cycles can be set by the user through the Nonvolatile and Volatile Configuration Registers (See the ***Table 9*** and ***Table 10***).

7.2.14 Dual Output Fast Read-DTR Sequence Diagram (3DH)

The Dual Output Fast Read-DTR (3DH) instruction (see the ***Figure 73-Figure 74***) allows for improved random access while maintaining two IO pins, IO0 and IO1. It is similar to the dual output fast Read (3BH) instruction, but has the ability to input address bits (A23/A31-0) and output data, two bits of data per clock.

The Dual Output Fast Read-DTR (3DH) instruction is supported in Extended SPI and Dual I/O SPI mode.

Figure 73. Dual Output Fast Read-DTR Sequence Diagram (Extended SPI Mode)

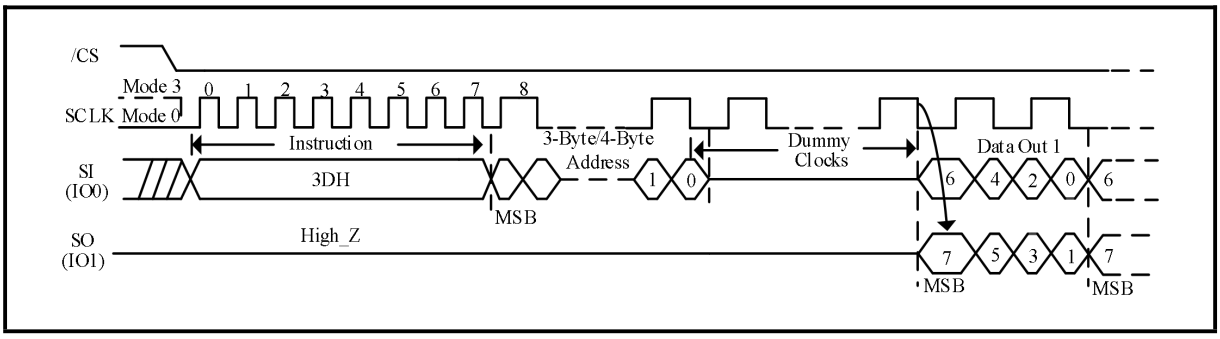
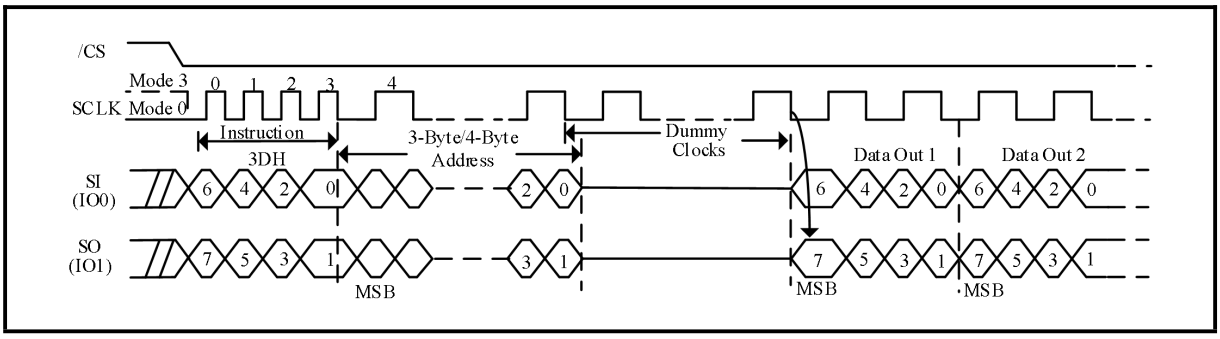


Figure 74. Dual Output Fast Read-DTR Sequence Diagram (Dual I/O Mode)



Note:

1. The Dual Output Fast Read-DTR instruction support 3-byte address and 4-byte address mode.
2. Dummy clock cycles can be set by the user through the Nonvolatile and Volatile Configuration Registers (See the ***Table 9*** and ***Table 10***).

7.2.15 Dual Input/Output Fast Read-DTR (BDH)

The Dual Input/Output Fast Read-DTR (BDH) instruction (see the ***Figure 75-Figure 76***) is similar to the Dual Output Fast Read-DTR (3DH) instruction but transfer the Address bits (A23/A31-0) is in IO0 and IO1 for Extended SPI protocol.

The Dual Output Fast Read-DTR (3DH) instruction is supported in Extended SPI and Dual I/O SPI mode.

Figure 75. Dual Input/Output Fast Read-DTR (Extended SPI Mode)

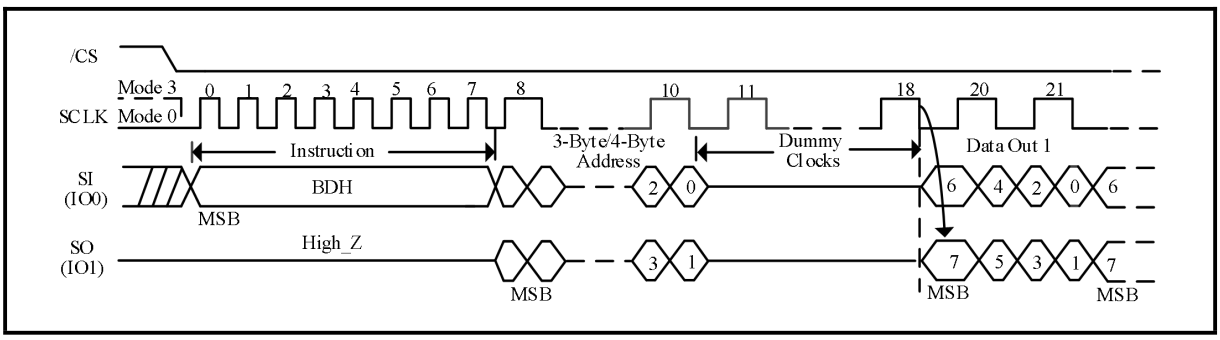
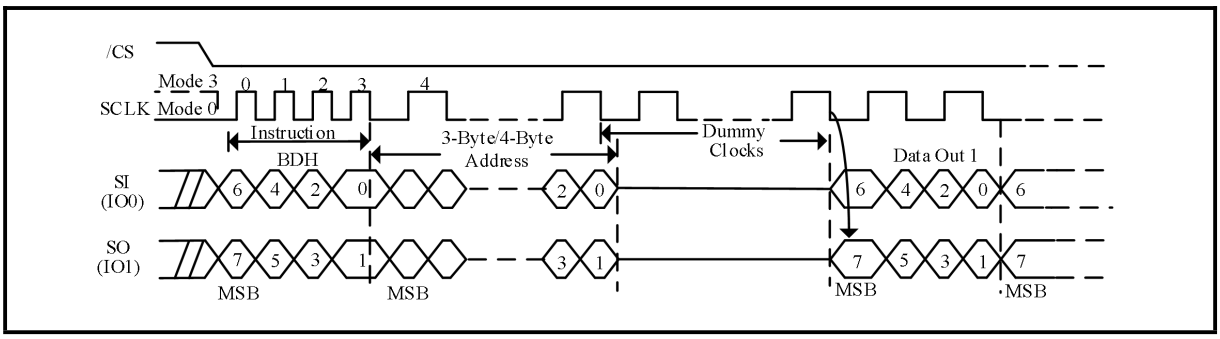


Figure 76. Dual Input/Output Fast Read-DTR (Dual I/O Mode)



Note:

1. The Dual Input/Output Fast Read-DTR instruction support 3-byte address and 4-byte address mode.
2. Dummy clock cycles can be set by the user through the Nonvolatile and Volatile Configuration Registers (See the ***Table 9*** and ***Table 10***).

7.2.16 Quad Output Fast Read-DTR (6DH)

The Quad Output Fast Read-DTR (6DH) instruction (see the ***Figure 77Figure 78***) is similar to the Quad Output Fast Read (6BH) instruction except that has the ability to input address bits (A23/A31-0) and output data, two bits of data per clock.

The Quad Output Fast Read-DTR (6DH) instruction is supported in Extended SPI and Quad I/O SPI mode.

Figure 77. Quad Output Fast Read-DTR (Extended SPI Mode)

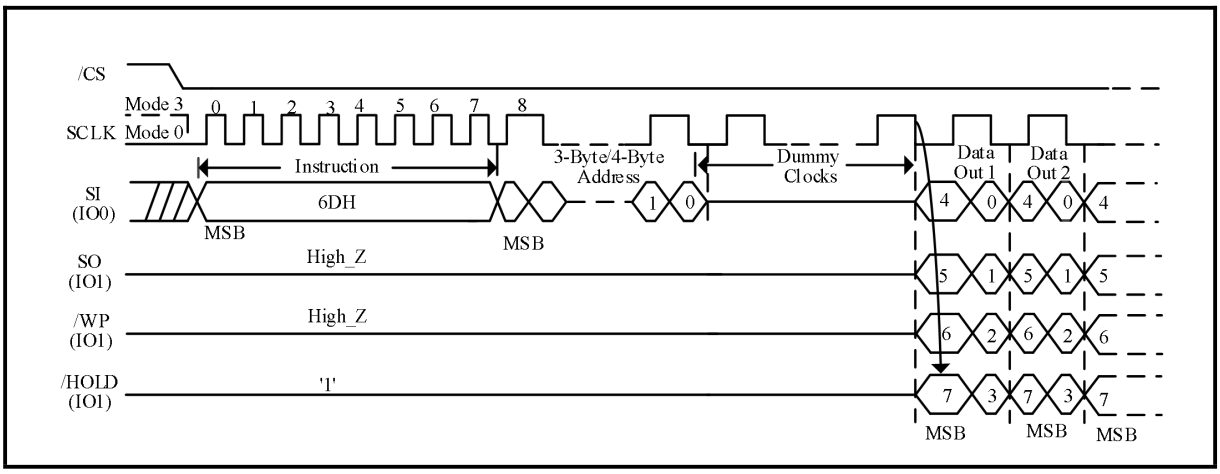
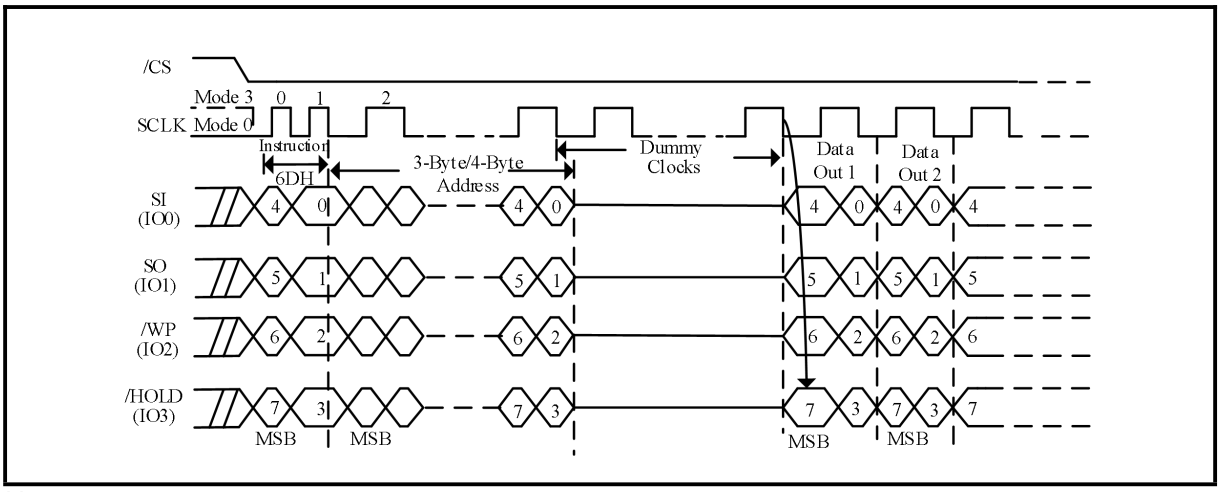


Figure 78. Quad Output Fast Read-DTR (Quad I/O Mode)



Note:

1. The Quad Output Fast Read-DTR instruction support 3-byte address and 4-byte address mode.
2. Dummy clock cycles can be set by the user through the Nonvolatile and Volatile Configuration Registers (See the ***Table 9*** and ***Table 10***).

7.2.17 Quad Input/Output Fast Read-DTR (EDH)

The Quad Input/Output Fast Read-DTR (EDH) instruction (see the ***Figure 79-Figure 80***) is similar to the Quad Output Fast Read-DTR (6DH) instruction but transfer the Address bits (A23/A31-0) is in IO0, IO1, IO2 and IO3 for Extended SPI protocol.

The Dual Input/Output Fast Read-DTR (EDH) instruction is supported in Extended SPI and Quad I/O SPI mode.

Figure 79. Quad Input/Output Fast Read-DTR (Extended SPI Mode)

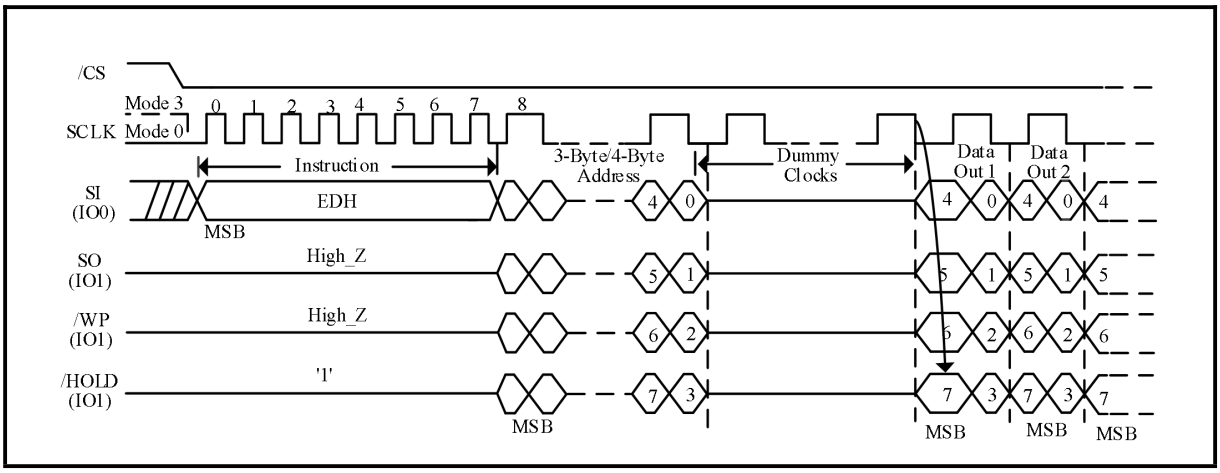
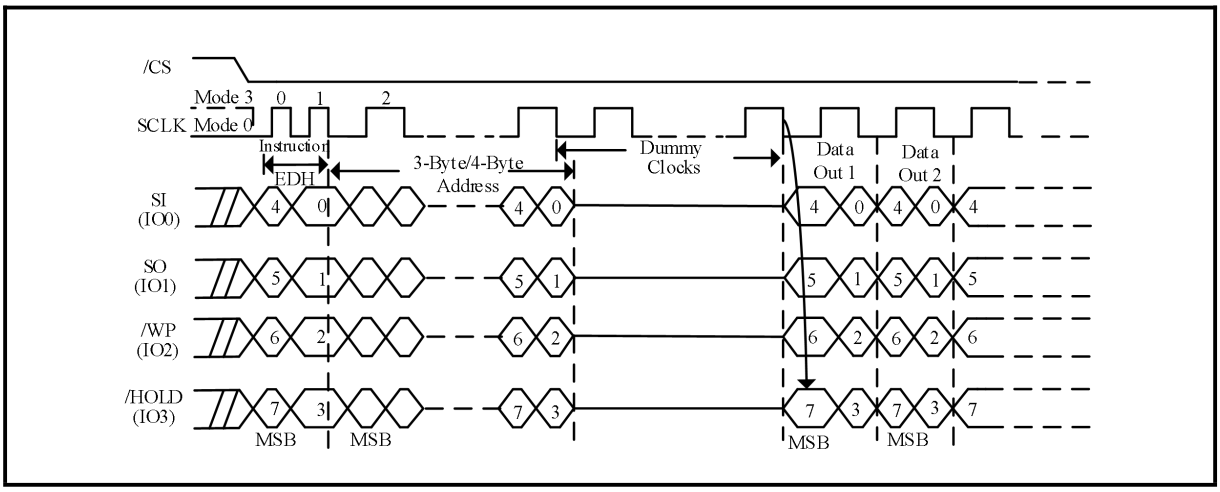


Figure 80. Quad Input/Output Fast Read-DTR (Quad I/O Mode)



Note:

1. The Quad Input/Output Fast Read-DTR instruction support 3-byte address and 4-byte address mode.
2. Dummy clock cycles can be set by the user through the Nonvolatile and Volatile Configuration Registers (See the ***Table 9*** and ***Table 10***).

7.3 Read Identification Instructions

7.3.1 Read ID (9E/9FH)and Multiple I/O Read ID（AFH）

See ***Figure 81***, the Read ID instruction provides users with the manufacturer ID, device ID and Unique ID assigned by JEDEC. /CS is driven low and the instruction code is input on SI. The device outputs the information seeing the ***Table 20***. When /CS is driven high, the device goes to standby. The operation is terminated by driving /CS HIGH at any time during data output.

See ***Figure 82-Figure 83,*** Multiple I/O Read ID instruction provides users with the manufacturer ID and device ID assigned by JEDEC, but does not include the Unique ID. /CS is driven low and the instruction code is input on IOn (for dual I/O protocol is SI-SO, quad I/O protocol is IO-IO3). The device outputs the information seeing the ***Table 20***. When /CS is driven high, the device goes to standby. The operation is terminated by driving /CS high at any time during data output.

At the same time, after outputting UID (Extended SPI Mode) or Device ID (Dual/Quad I/O Mode), if continue to send SCLK, the output data is “don’t care”.

If an Erase or Program cycle is in progress when the instruction is executed, the instruction is not decoded and the instruction cycle in progress is not affected.

Figure 81. Figure Read ID instruction (Extended SPI Mode)

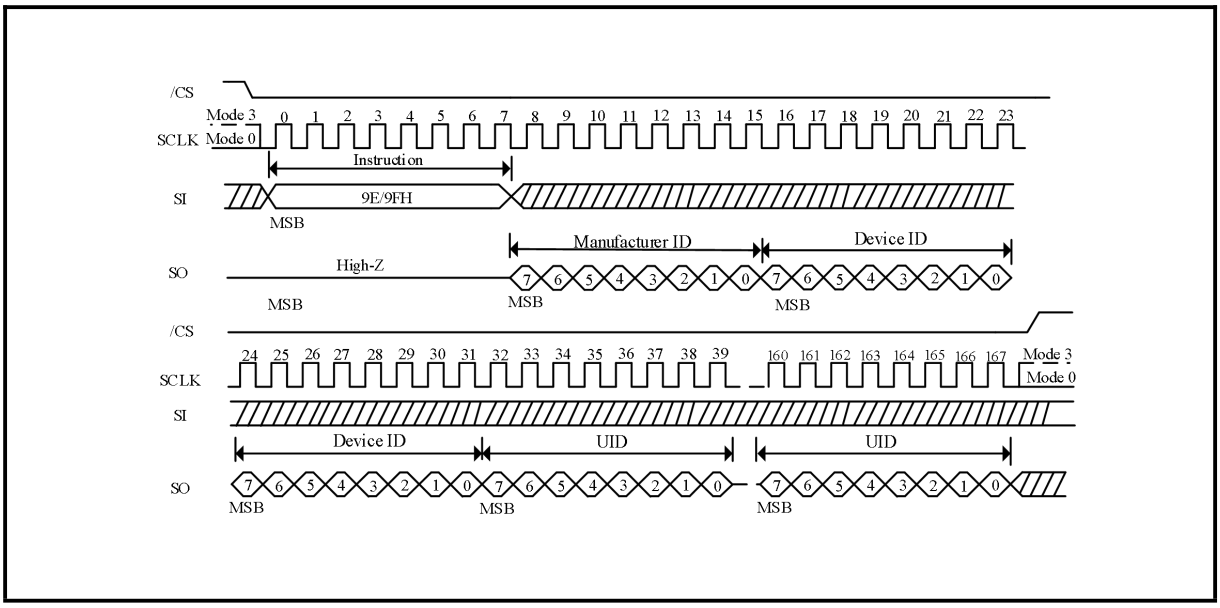


Figure 82. Multiple I/O Read ID instruction (Dual I/O Mode)

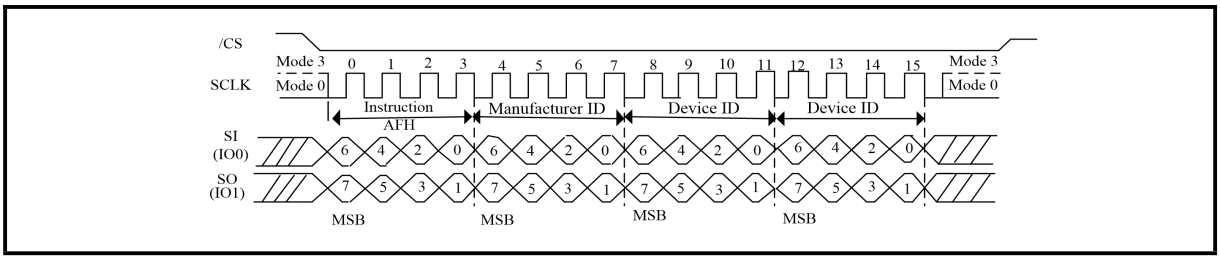
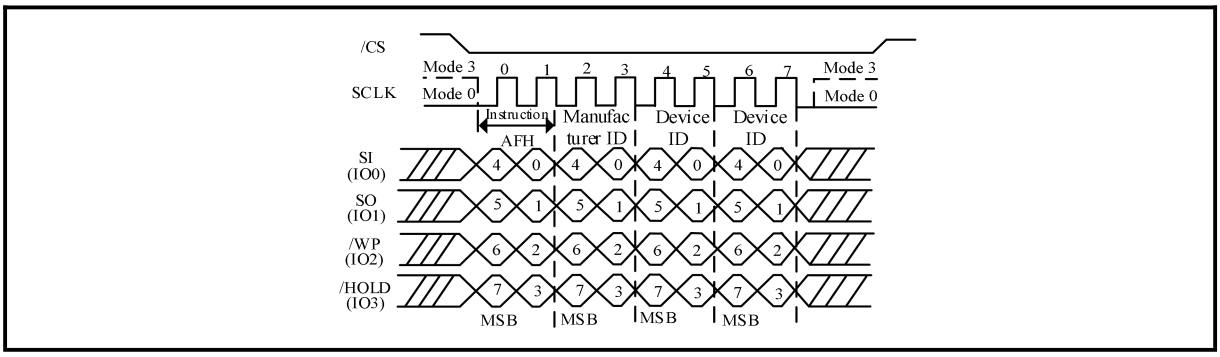


Figure 83. Multiple I/O Read ID (Quad I/O Mode)



Note:

1. The Read ID instruction is represented by the extended SPI protocol timing shown first.
2. The Multiple I/O Read ID instruction is represented by the dual and quad SPI protocols are shown below extended SPI protocol.

7.3.2 Read Serial Flash Discovery Parameter (5AH)

To execute Read Serial Flash Discovery Parameter instruction (See ***Figure 84-Figure 86***),/CS is driven low. The instruction code is input on SI, followed by three address bytes and eight dummy clock cycles (address is always 3 bytes, even if the device is configured to work in 4-byte address mode). The device outputs the information starting from the specified address. When the 2048-byte boundary is reached, the data output wraps to address 0 of the serial Flash discovery parameter table, seeing the ***Appendix***. The operation is terminated by driving /CS high at any time during data output.

The operation always executes in continuous mode so the Read burst wrap setting in the volatile configuration register does not apply.

Figure 84. Read Serial Flash Discovery Parameter instruction (Extended SPI Mode)

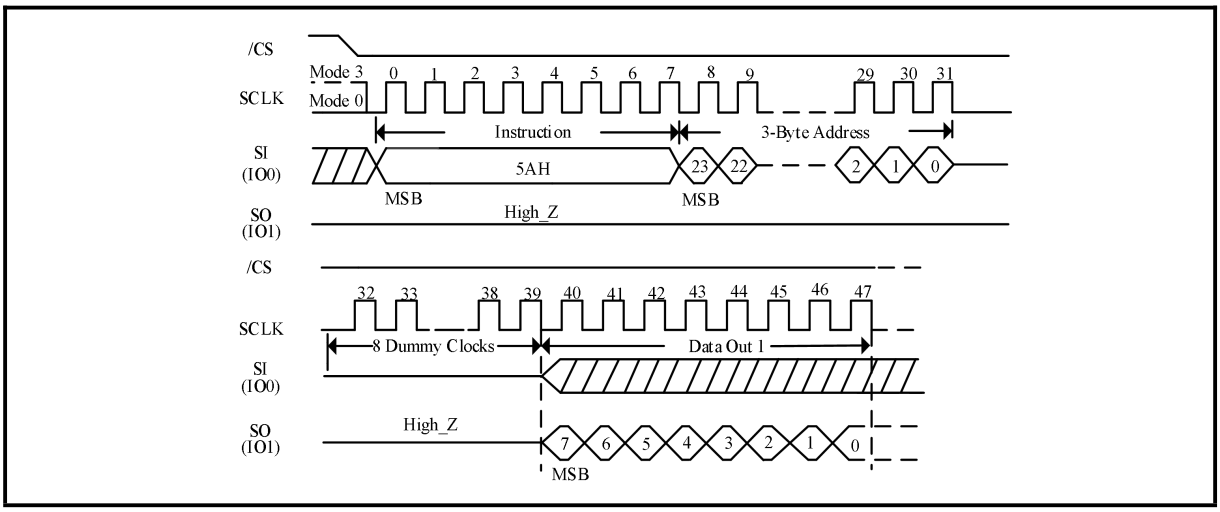


Figure 85. Read Serial Flash Discovery Parameter instruction (Dual I/O Mode)

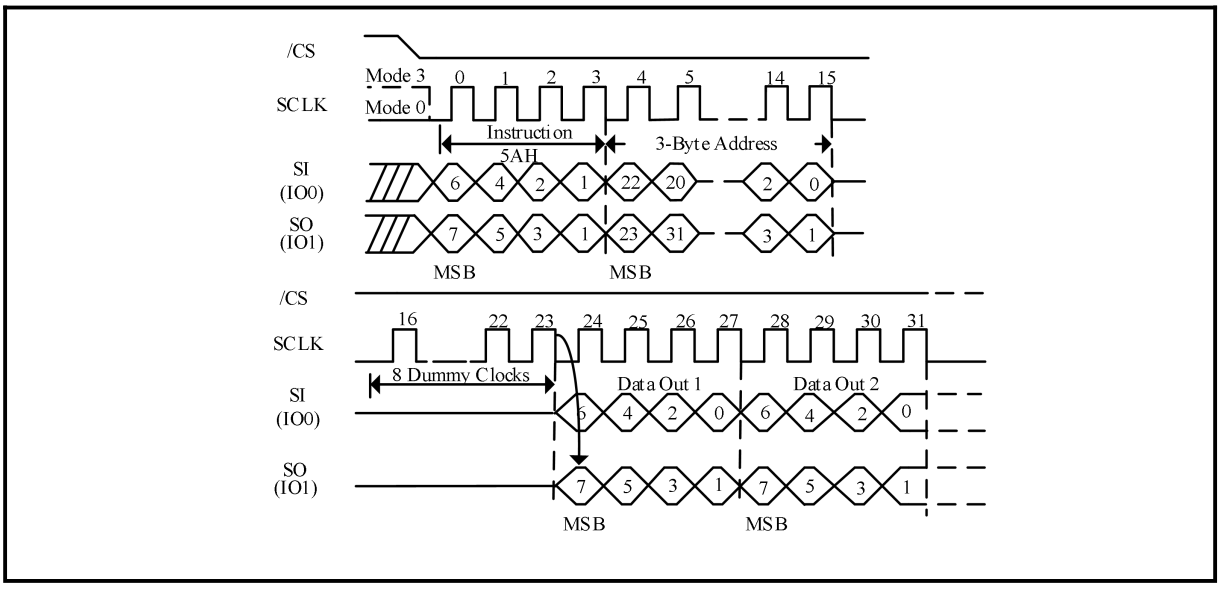
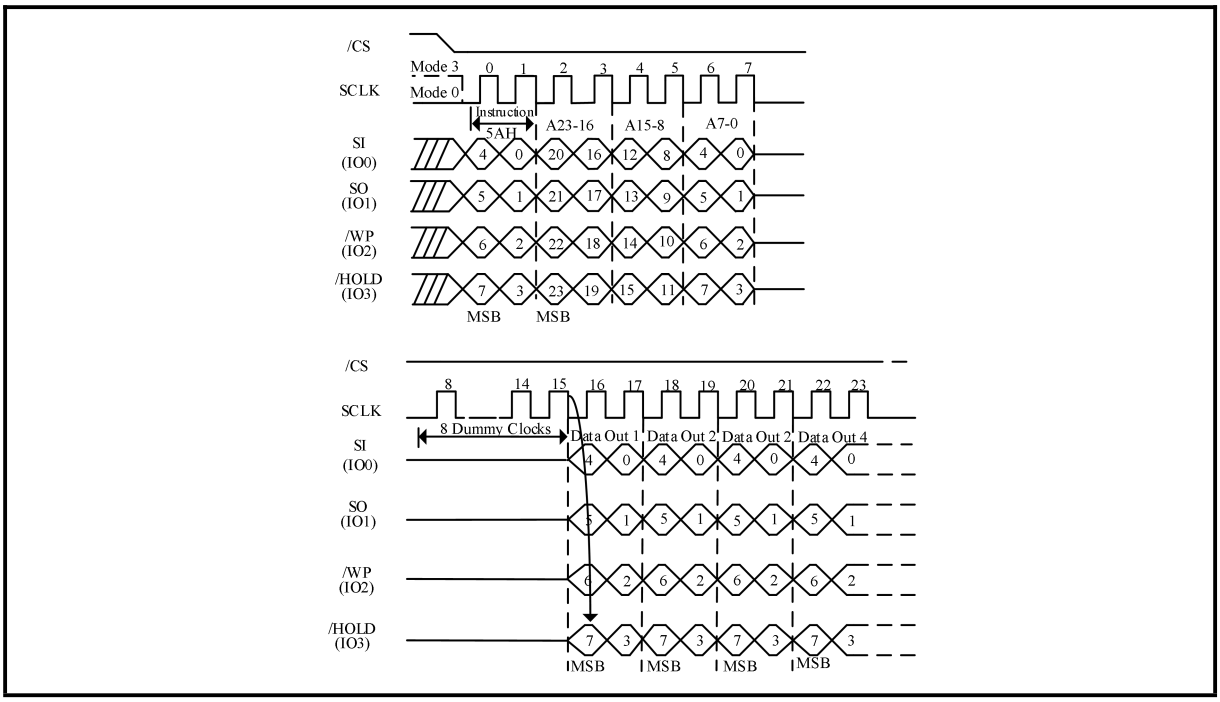


Figure 86. Read Serial Flash Discovery Parameter (Quad I/O Mode)



7.4 Program and Erase Instructions

7.4.1 Page Program (02H)

The Page Program instruction is for programming the memory. A Write Enable instruction must previously have been executed to set the Write Enable Latch bit to 1 before sending the Page Program instruction. See ***Figure 87-Figure 89***, the Page Program instruction is entered by driving /CS low, followed by the instruction code, 3-byte or 4-byte address and at least one data byte on SI (for dual I/O protocol is IO0-IO1, quad I/O protocol is IO-IO3). Each address bit is latched in during the rising edge of the clock. When /CS is driven high, the operation, which is self-timed, is initiated; its duration is tPP.

If the bits of the least significant address, which is the starting address, are not all zero, all data transmitted beyond the end of the current page is Programmed from the starting address of the same page. If the number of bytes sent to the device exceed the maximum page size, previously latched data is discarded and only the last maximum page size number of data bytes are guaranteed to be Programmed correctly within the same page. If the number of bytes sent to the device is less than the maximum page size, they are correctly programmed at the specified addresses without any effect on the other bytes of the same page.

/CS must be driven low for the entire duration of the sequence. The Page Program instruction sequence: /CS goes low-> sending Page Program instruction ->3-byte or 4-byte address on SI (for dual I/O protocol is IO0-IO1, quad I/O protocol is IO-IO3) ->at least 1 byte data on SI (for dual I/O protocol is IO0-IO1, quad I/O protocol is IO-IO3) -> /CS goes high.

When the operation is in progress, the Program or erase controller bit of the flag status register is set to 0. The write enable latch bit is cleared to 0, whether the operation is successful or not. The status register and flag status register can be polled for the operation status. The operation is considered complete after bit 7 of the flag status register outputs 1 with at least one byte output. When the operation completes, the Program or erase controller bit is cleared to 1.

If the operation times out, the write enable latch bit is reset and the Program fail bit is set to 1. If /CS is not driven high the instruction is not executed, flag status register error bits are not set, and the write enable latch remains set to 1. When a instruction is applied to a protected sector, the instruction is not executed, the write enable latch bit remains set to 1, and flag status register bits 1 and 4 are set.

Note:

1. The flag status register must be polled even if operation times out.

Figure 87. Page Program Sequence Diagram (Extended SPI Mode)

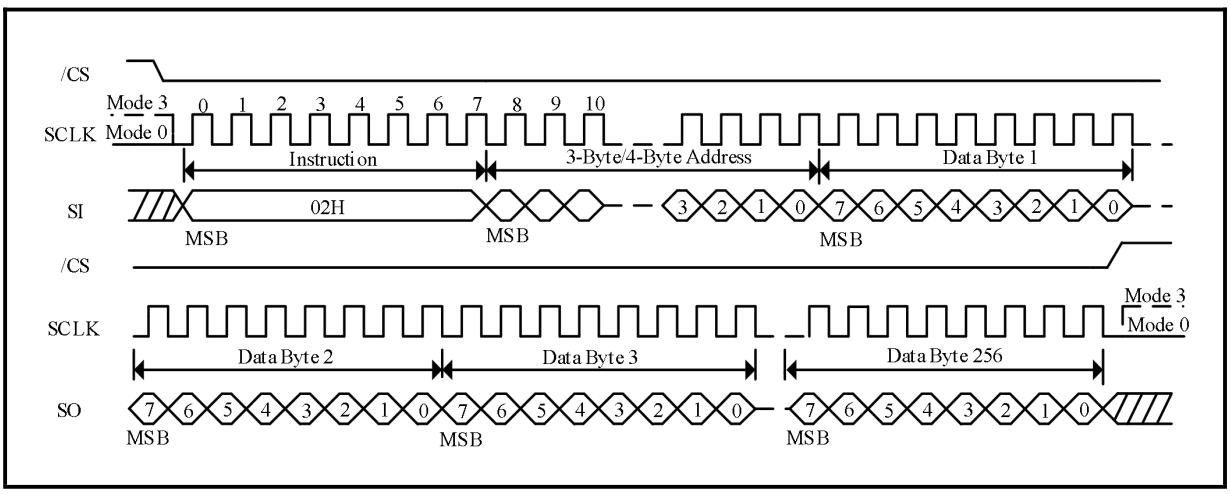


Figure 88. Page Program Sequence Diagram (Dual I/O Mode)

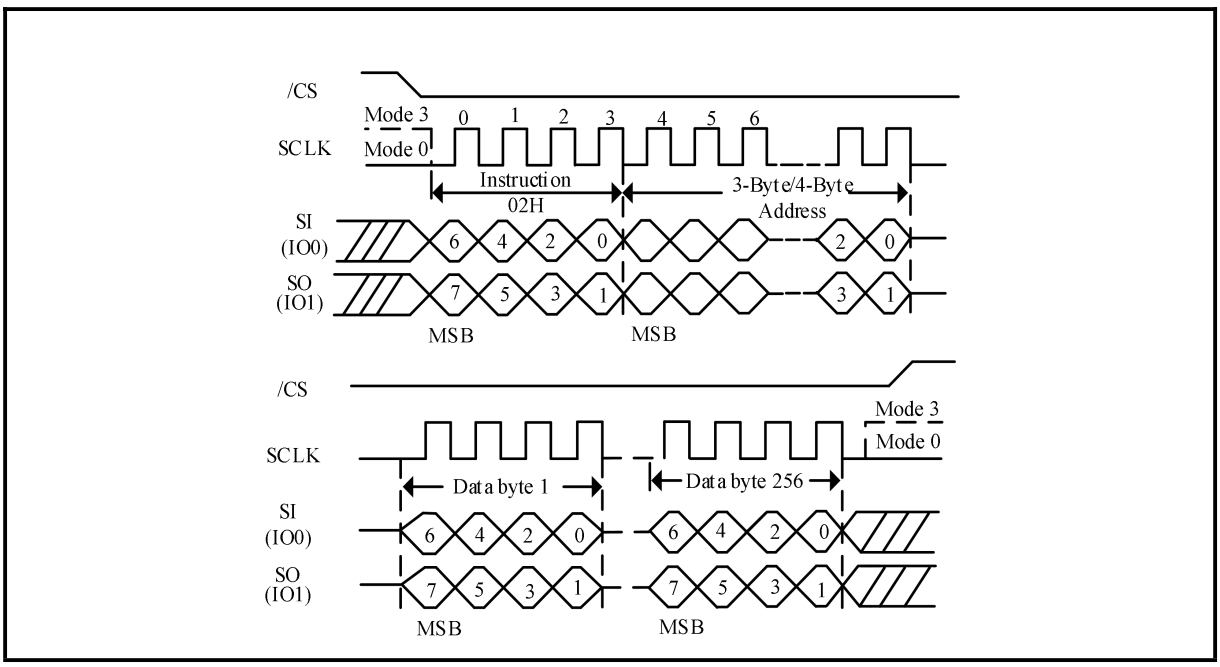
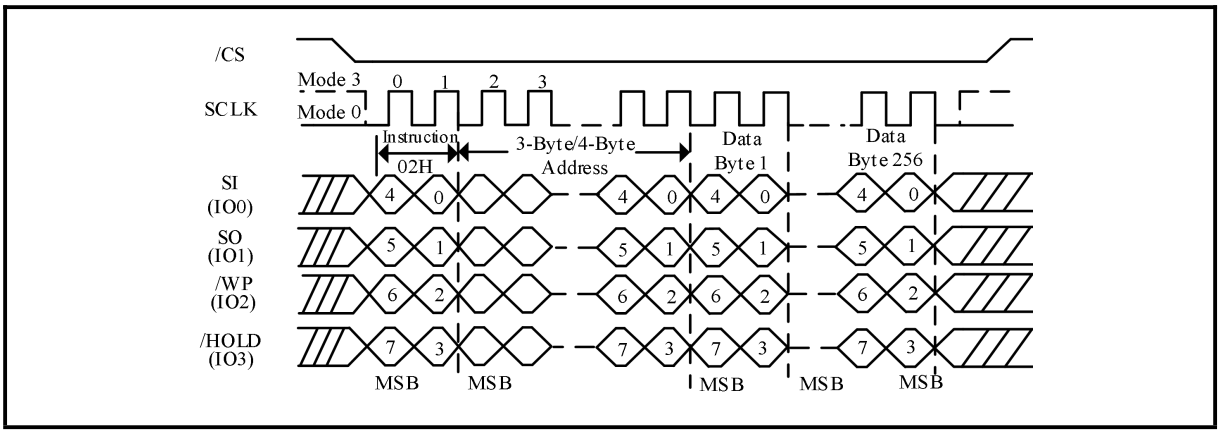


Figure 89. Page Program Sequence Diagram (Quad I/O Mode)



Note:

1. The Page Program instruction support 3-byte address and 4-byte address mode.

7.4.2 Dual Input Fast Program (A2H)

The Dual Input Fast Program instruction are initiated by first executing the Write Enable instruction to set the Write Enable Latch bit to 1. The Dual Input Fast Program instruction (see ***Figure 90-Figure 91***) is for programming the memory using for pins: IO0 and IO1. This instruction supports Extended SPI protocol and dual SPI protocol. The Dual Input Fast Program instruction is entered by driving /CS low, followed by the instruction code (A2H), 3-byte or 4-byte bytes address and at least one data byte on IO pins.

When the operation is in progress, the program or erase controller bit of the flag status register is set to 0. The write enable latch bit is cleared to 0, whether the operation is successful or not. The status register and flag status register can be polled for the operation status. The operation is considered complete after bit 7 of the flag status register outputs 1 with at least one byte output. When the operation completes, the program or erase controller bit is cleared to 1.

If the operation times out, the write enable latch bit is reset and the Program fail bit is set to 1. If /CS is not driven high the instruction is not executed, flag status register error bits are not set, and the write enable latch remains set to 1. When a instruction is applied to a protected sector, the instruction is not executed, the write enable latch bit remains set to 1, and flag status register bits 1 and 4 are set.

Figure 90. Dual Input Fast Program Sequence Diagram (Extended SPI Mode)

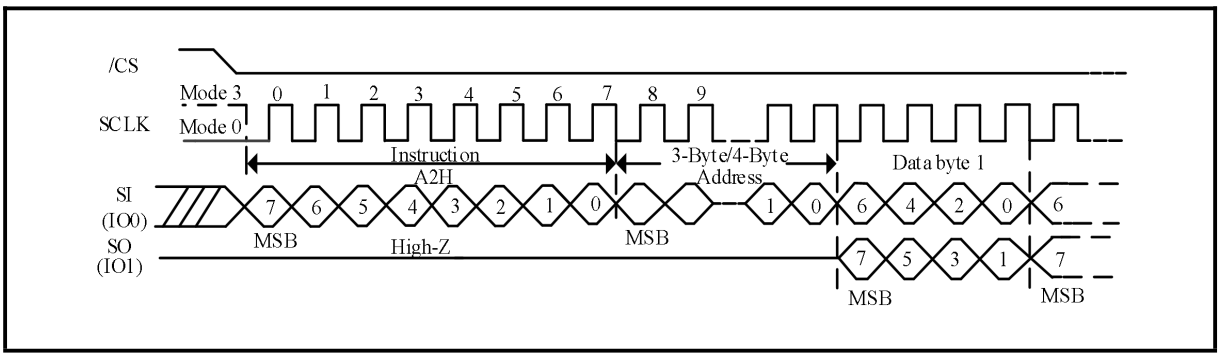
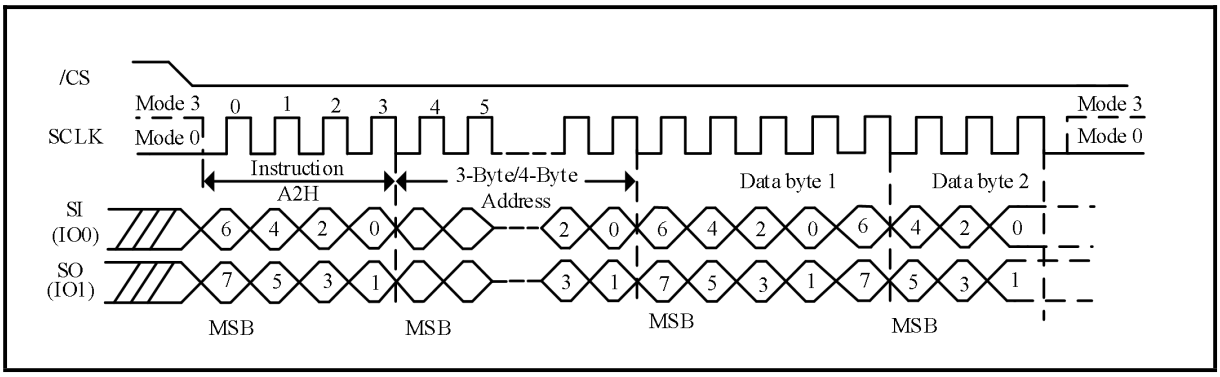


Figure 91. Dual Input Fast Program Sequence Diagram (Dual I/O Mode)



Note:

1. The Dual Input Fast Program instruction support 3-byte address and 4-byte address mode.

7.4.3 Extended Dual Input Fast Program (D2H)

The Extended Dual Input Fast Program instruction is similar to the Dual Input Fast Program instruction except that it requires address transfer in IO0 and IO1. The Extended Dual Input Fast Program instruction are initiated by first executing the Write Enable instruction to set the Write Enable Latch bit to 1. The Extended Dual Input Fast Program instruction (see ***Figure 92-Figure 93***) is for programming the memory using for pins: IO0 and IO1. This instruction supports Extended SPI protocol and dual SPI protocol. The Extended Dual Input Fast Program instruction is entered by driving /CS Low, followed by the instruction code (D2H), 3-byte or 4-byte bytes address and at least one data byte on IO pins.

When the operation is in progress, the program or erase controller bit of the flag status register is set to 0. The write enable latch bit is cleared to 0, whether the operation is successful or not. The status register and flag status register can be polled for the operation status. The operation is considered complete after bit 7 of the flag status register outputs 1 with at least one byte output. When the operation completes, the program or erase controller bit is cleared to 1.

If the operation times out, the Write Enable Latch bit is reset and the Program fail bit is set to 1. If /CS is not driven high the instruction is not executed, flag status register error bits are not set, and the write enable latch remains set to 1. When a instruction is applied to a protected sector, the instruction is not executed, the write enable latch bit remains set to 1, and flag status register bits 1 and 4 are set.

Figure 92. Extended Dual Input Fast Program (Extended SPI Mode)

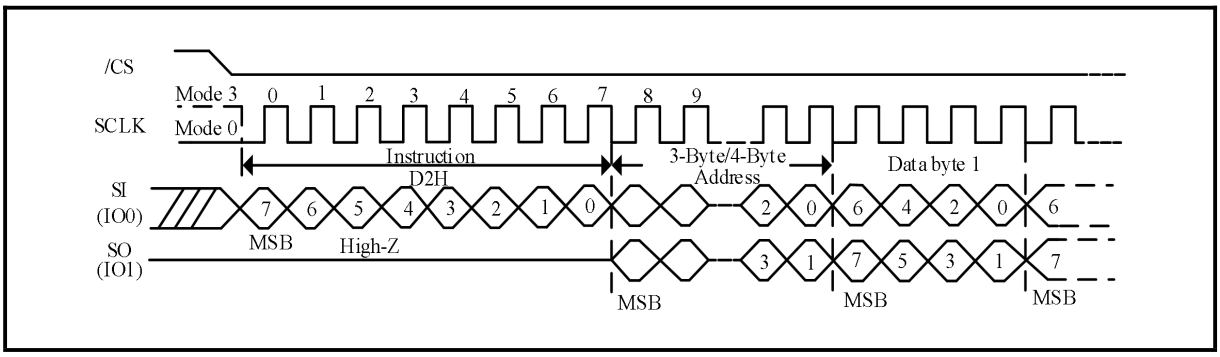
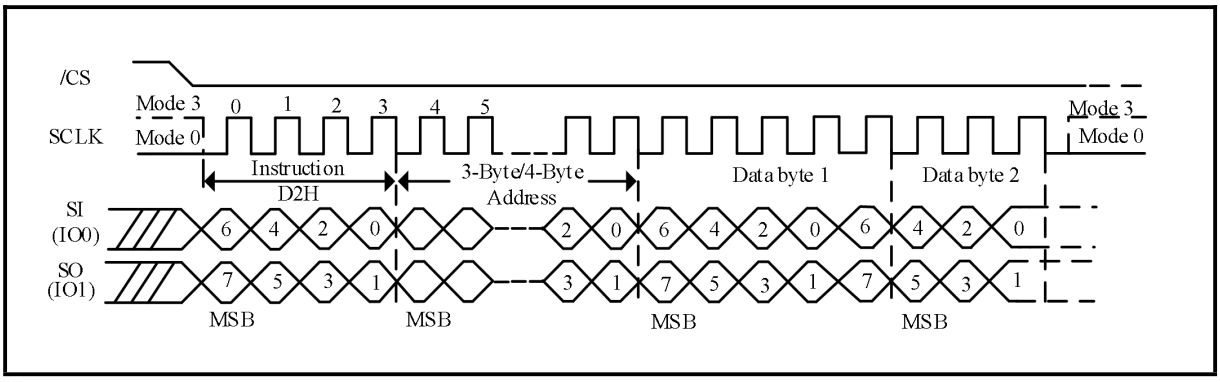


Figure 93. Extended Dual Input Fast Program (Dual I/O Mode/3-Byte Mode)



Note:

1. The Extended Dual Input Fast Program instruction support 3-byte address and 4-byte address mode.

7.4.4 Quad Input Fast Program (32H)

The Quad Input Fast Program instruction are initiated by first executing the Write Enable instruction to set the Write Enable Latch bit to 1. The Dual Input Fast Program instruction (see ***Figure 94-Figure 95***) is for programming the memory using for pins: IO0, IO1, IO2 and IO3. This instruction supports Extended SPI protocol and quad SPI protocol. The Quad Input Fast Program instruction is entered by driving /CS low, followed by the instruction code (32H), 3-byte or 4-byte address bytes and at least one data byte on IO pins.

When the operation is in progress, the program or erase controller bit of the flag status register is set to 0. The write enable latch bit is cleared to 0, whether the operation is successful or not. The status register and flag status register can be polled for the operation status. The operation is considered complete after bit 7 of the flag status register outputs 1 with at least one byte output. When the operation completes, the program or erase controller bit is cleared to 1.

If the operation times out, the Write Enable Latch bit is reset and the Program fail bit is set to 1. If /CS is not driven high the instruction is not executed, flag status register error bits are not set, and the write enable latch remains set to 1. When a instruction is applied to a protected sector, the instruction is not executed, the write enable latch bit remains set to 1, and flag status register bits 1 and 4 are set.

Figure 94. Quad Input Fast Program (Extended SPI Mode)

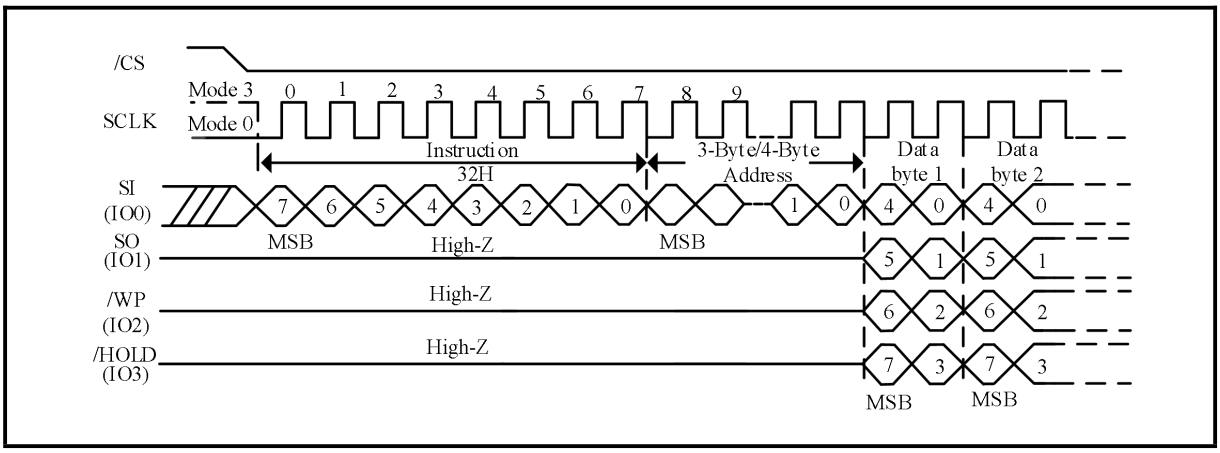
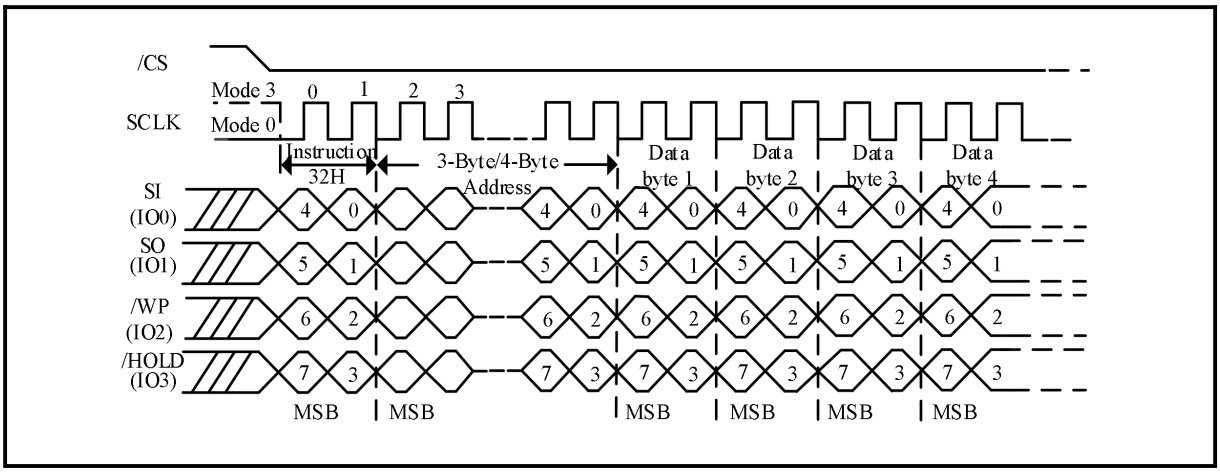


Figure 95. Quad Input Fast Program (Quad I/O Mode)



Note:

1. The Quad Input Fast Program instruction support 3-byte address and 4-byte address mode.

7.4.5 Extended Quad Input Fast Program (12H)

The Extended Quad Input Fast Program instruction is similar to the Dual Input Fast Program instruction except that it requires address transfer in IO0, IO1, IO2 and IO3. The Quad Input Fast Program instruction are initiated by first executing the Write Enable instruction to set the Write Enable Latch bit to 1. The Dual Input Fast Program instruction (see ***Figure 96-Figure 97***) is for programming the memory using for pins: IO0, IO1, IO2 and IO3. This instruction supports Extended SPI protocol and quad SPI protocol. The Quad Input Fast Program instruction is entered by driving /CS Low, followed by the instruction code (12H), 3-byte or 4-byte address bytes and at least one data byte on IO pins.

When the operation is in progress, the program or erase controller bit of the flag status register is set to 0. The write enable latch bit is cleared to 0, whether the operation is successful or not. The status register and flag status register can be polled for the operation status. The operation is considered complete after bit 7 of the flag status register outputs 1 with at least one byte output. When the operation completes, the program or erase controller bit is cleared to 1.

If the operation times out, the Write Enable Latch bit is reset and the Program fail bit is set to 1. If /CS is not driven high the instruction is not executed, flag status register error bits are not set, and the write enable latch remains set to 1. When a instruction is applied to a protected sector, the instruction is not executed, the write enable latch bit remains set to 1, and flag status register bits 1 and 4 are set.

Figure 96. Extended Quad Input Fast Program (Extended SPI Mode)

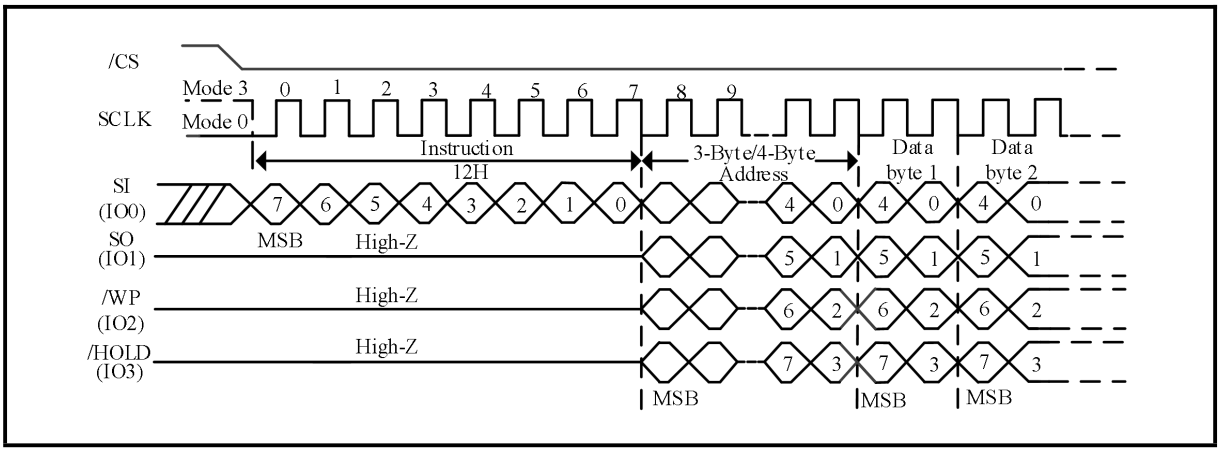
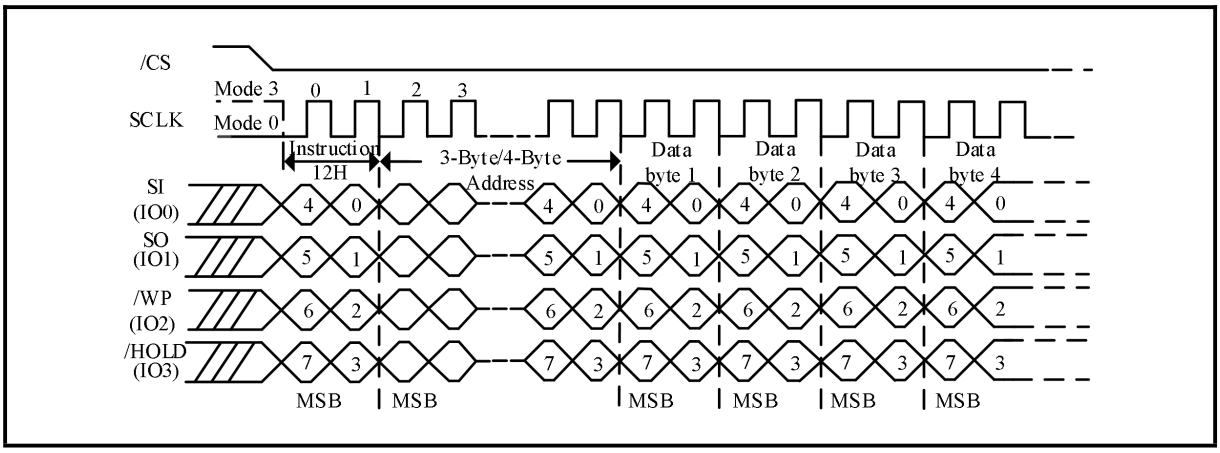


Figure 97. Extended Quad Input Fast Program (Quad I/O Mode)



Note:

1. The Extended Quad Input Fast Program instruction support 3-byte address and 4-byte address mode.

7.4.6 Subsector Erase (20H)

The Subsector Erase instruction is for erasing the all data of the chosen Subsector. A Write Enable instruction must previously have been executed to set the Write Enable Latch bit. The Subsector Erase instruction (see ***Figure 98-Figure 100***) is entered by driving /CS low, followed by the instruction code, and address byte on IO pin. Any address inside the subsector is a valid address for the Subsector Erase instruction. /CS must be driven low for the entire duration of the sequence. Each address bit is latched in during the rising edge of the clock. When /CS is driven HIGH, the operation, which is self-timed, is initiated; its duration is tSSE. The operation can be suspended and resumed by the Program/Erase Suspend and Program/Erase Resume instructions, respectively.

If the Write Enable Latch bit is not set, the device ignores the Subsector Erase instruction and no error bits are set to indicate operation failure.

When the operation is in progress, the Program or erase controller bit is set to 0. The Write Enable Latch bit is cleared to 0, whether the operation is successful or not. The status register and flag status register can be polled for the operation status. The operation is considered complete once bit 7 of the flag status register outputs 1 with at least one byte output. When the operation completes, the Program or erase controller bit is cleared to 1.

If the operation times out, the write enable latch bit is reset and the erase error bit is set to 1. If /CS is not driven HIGH, the instruction is not executed, flag status register error bits are not set, and the write enable latch remains set to 1. When a instruction is applied to a protected subsector, the instruction is not executed. Instead, the write enable latch bit remains set to 1, and flag status register bits 1 and 5 are set.

Note: that the flag status register must be polled even if operation times out.

Figure 98. Subsector Erase Sequence Diagram (Extended SPI Mode)

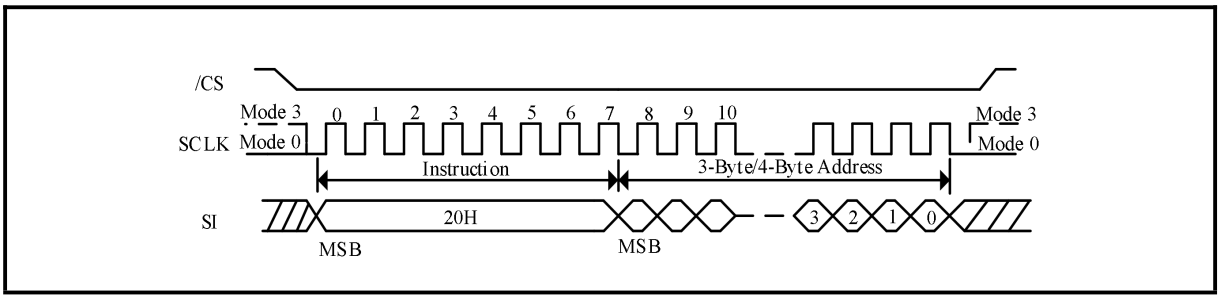


Figure 99. Subsector Erase Sequence Diagram (Dual I/O Mode)

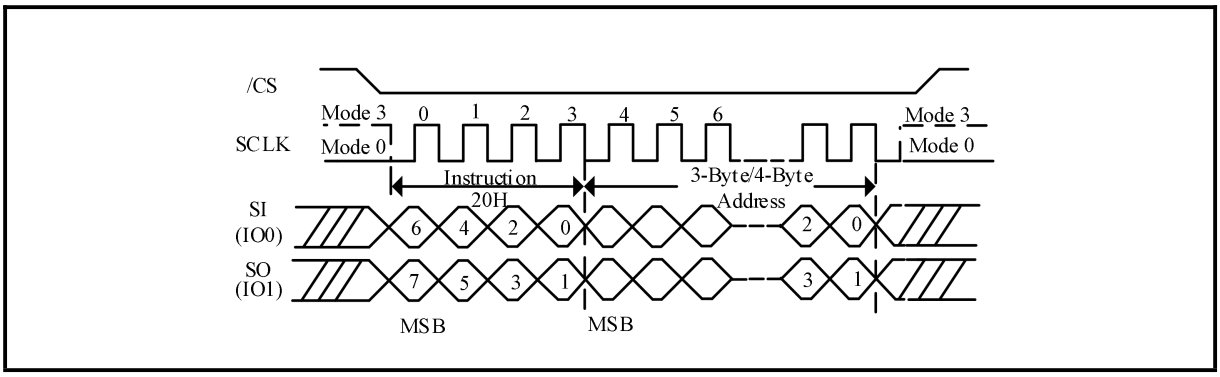
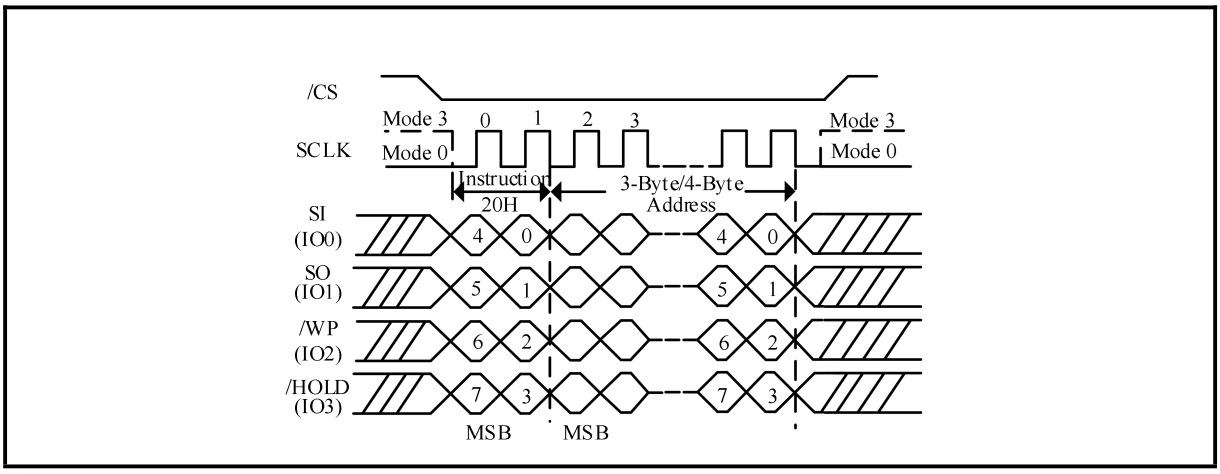


Figure 100. Subsector Erase Sequence Diagram (Quad I/O Mode)



Note:

1. The Subsector Erase instruction support 3-byte address and 4-byte address mode.

7.4.7 Sector Erase (D8H)

The Sector Erase instruction is for erasing the all data of the chosen Sector. A Write Enable instruction must previously have been executed to set the Write Enable Latch bit. The Sector Erase instruction (see ***Figure 101-Figure 103***) is entered by driving /CS low, followed by the instruction code, and address byte on IO pin. Any address inside the sector is a valid address for the Sector Erase instruction. /CS must be driven low for the entire duration of the sequence. Each address bit is latched in during the rising edge of the clock. When /CS is driven HIGH, the operation, which is self-timed, is initiated; its duration is tSE. The operation can be suspended and resumed by the Program/Erase Suspend and Program/Erase Resume instructions, respectively.

If the write enable latch bit is not set, the device ignores the Sector Erase instruction and no error bits are set to indicate operation failure.

When the operation is in progress, the program or erase controller bit is set to 0. The write enable latch bit is cleared to 0, whether the operation is successful or not. The status register and flag status register can be polled for the operation status. The operation is considered complete once bit 7 of the flag status register outputs 1 with at least one byte output. When the operation completes, the program or erase controller bit is cleared to 1.

If the operation times out, the write enable latch bit is reset and erase error bit is set to 1. If /CS is not driven HIGH, the instruction is not executed, flag status register error bits are not set, and the write enable latch remains set to 1. When a instruction is applied to a protected sector, the instruction is not executed. Instead, the write enable latch bit remains set to 1, and flag status register bits 1 and 5 are set.

Note: that the flag status register must be polled even if operation times out.

Figure 101. Sector Erase Sequence Diagram (Extended SPI Mode)

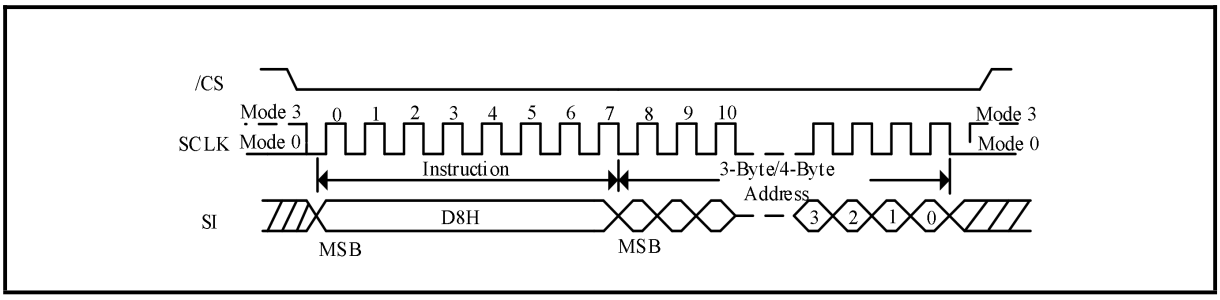


Figure 102. Sector Erase Sequence Diagram (Dual I/O Mode)

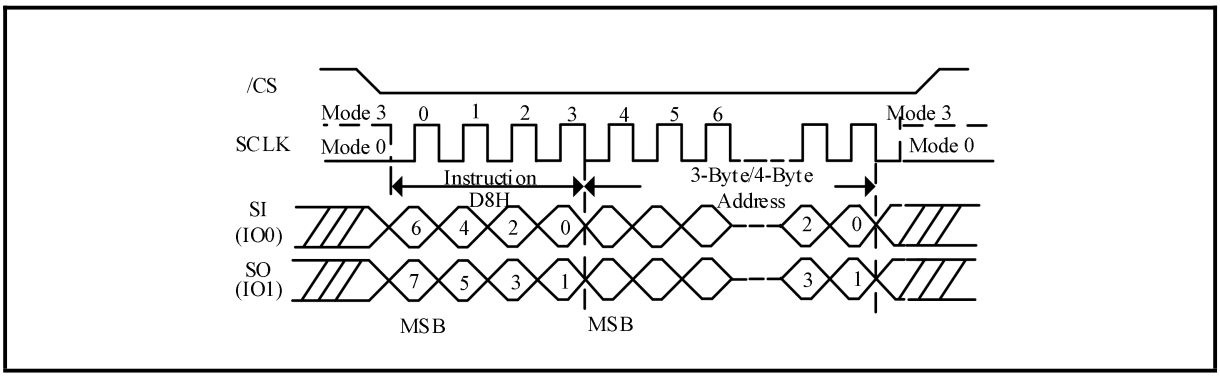
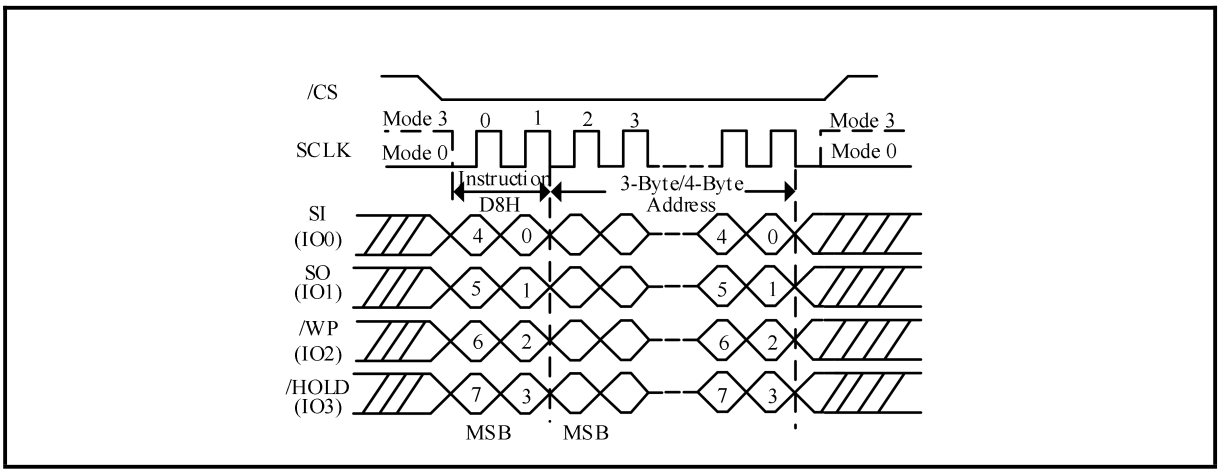


Figure 103. Sector Erase Sequence Diagram (Quad I/O SPI Mode)



Note:

1. The Subsector Erase instruction support 3-byte address and 4-byte address mode.

7.4.8 Die Erase (C4H)

The Die Erase instruction is for erasing the all data of the chosen Sector. A Write Enable instruction must previously have been executed to set the Write Enable Latch bit. The Sector Erase instruction (see ***Figure 104-Figure 106***) is entered by driving /CS low, followed by the instruction code, and address byte on IO pin. Any address inside the single 256Mb die is a valid address for the Die Erase instruction. /CS must be driven low for the entire duration of the sequence. Each address bit is latched in during the rising edge of the clock. When /CS is driven HIGH, the operation, which is self-timed, is initiated; its duration is tDSE.

If the write enable latch bit is not set, the device ignores the DIE ERASE instruction and no error bits are set to indicate operation failure.

When the operation is in progress, the program or erase controller bit is set to 0. The write enable latch bit is cleared to 0, whether the operation is successful or not. The status register and flag status register can be polled for the operation status. The operation is considered complete once

bit 7 of the flag status register outputs 1 with at least one byte output. When the operation completes, the program or erase controller bit is cleared to 1.

The instruction is not executed if any sector is locked. Instead, the write enable latch bit remains set to 1, and flag status register bits 1 and 5 are set.

Figure 104. Die Erase Sequence Diagram (Extended SPI Mode)

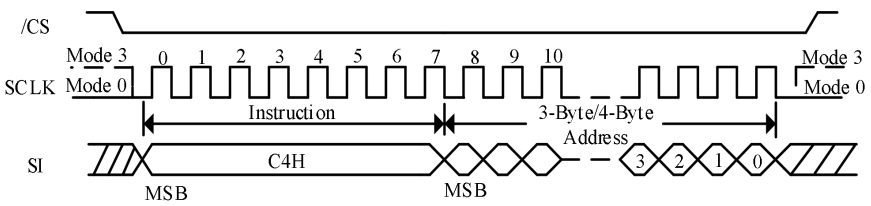


Figure 105. Die Erase Sequence Diagram (Dual I/O Mode)

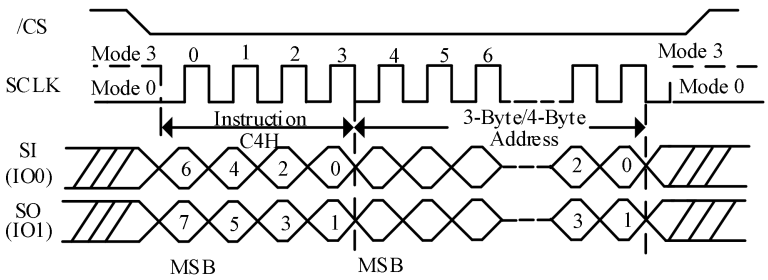
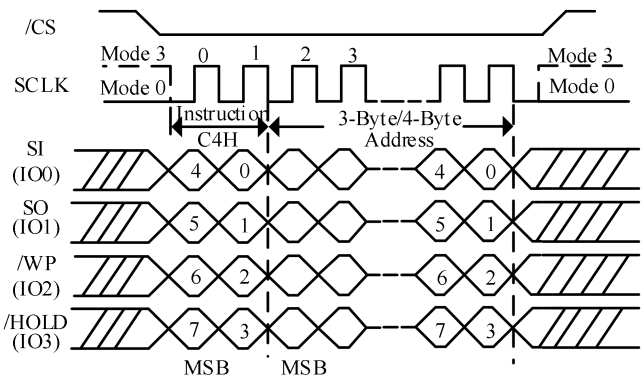


Figure 106. Die Erase Sequence Diagram (Quad I/O Mode)



Note:

1. The Subsector Erase instruction support 3-byte address and 4-byte address mode.

7.4.9 Program/Erase Suspend (75H)

The Program/Erase Suspend instruction allows the system to interrupt a Subsector or Sector Erase operation, then Read from or program data to any other sector. The Program/Erase Suspend instruction also allows the system to interrupt a Page Program operation and then Read from any other page or erase any other sector or block. To initiate the Program/Erase Suspend instruction, /CS is driven low. The instruction code is input on SI (for dual I/O protocol is IO0-IO1, quad I/O protocol is IO-IO3). The operation is terminated by the Program/Erase Resume instruction. The Program/Erase Suspend instruction sequence is shown in ***Figure 107-Figure 108***.

If a Suspend instruction is issued during a Program operation, then the flag status register bit 2 is set to 1. After Program/Erase latency time, the flag status register bit 7 is also set to 1, but the device is considered in suspended state once bit 7 of the flag status register outputs 1 with at least one byte output. In the suspended state, the device is waiting for any operation (See the ***Table 25***).

If a Suspend instruction is issued during an Erase operation, then the flag status register bit 6 is set to 1. After erase/Program latency time, the flag status register bit 7 is also set to 1, but the device is considered in suspended state once bit 7 of the flag status register outputs 1 with at least one byte output. In the suspended state, the device is waiting for any operation (See the ***Table 25***).

If the time remaining to complete the operation is less than the suspend latency, the device completes the operation and clears the flag status register bits 2 or 6, as applicable. Because the suspend state is volatile, if there is a power cycle, the Suspend state information is lost and the flag status register powers up as 80h.

During an Erase Suspend operation, a Program or Read operation is possible in any sector except the one in a suspended state. Reading from a sector that is in a suspended state will output indeterminate data. The device ignores a PROGRAM instruction to a sector that is in an erase suspend state; it also sets the flag status register bit 4 to 1, Program failure/protection error, and leaves the write enable latch bit unchanged. The instructions allowed during an erase suspend state are shown in the ***Table 25***. When the Erase resumes, it does not check the new lock status of the Write Lock Register instruction.

During a Program Suspend operation, a Read operation is possible in any page except the one in a suspended state. Reading from a page that is in a suspended state will output indeterminate data. The instructions allowed during a Program suspend state include the Write Volatile Configuration Register instruction and the Write Enhanced Volatile Configuration Register instruction.

It is possible to nest a Program/Erase Suspend operation inside a Program/Erase Suspend operation just once. Issue an Erase instruction and suspend it. Then issue a Program instruction and suspend it also. With the two operations suspended, the next Program/Erase Resume instruction resumes the latter operation, and a second Program/Erase Resume instruction resumes the former (or first) operation.

Figure 107. Program/Erase Suspend (Extended SPI Mode)

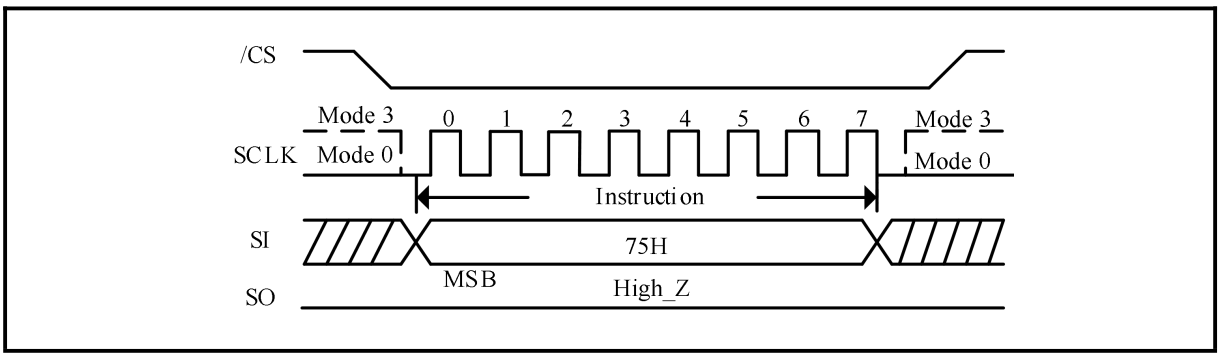


Figure 108. Program/Erase Suspend (Dual/Quad I/O Mode)

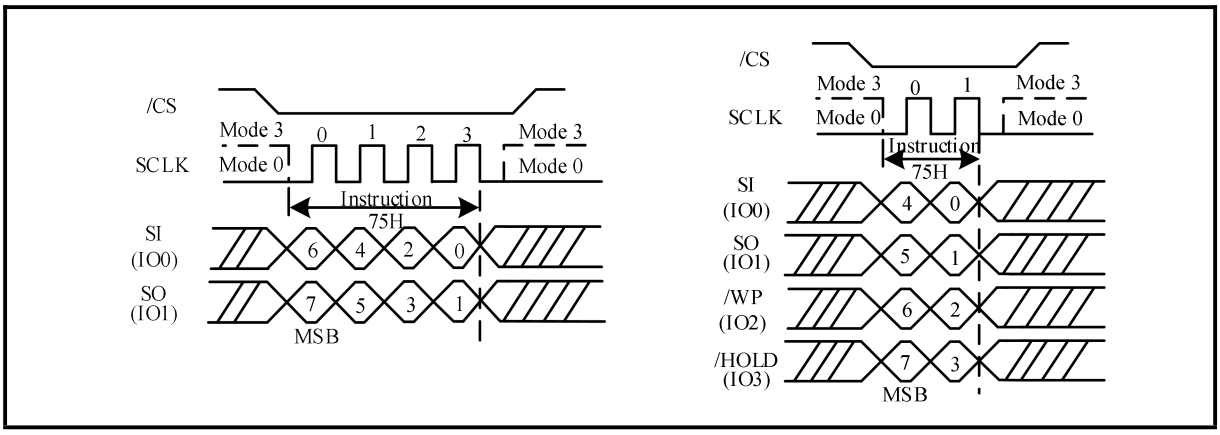


Table 24. Suspend Parameters

Parameter	Condition	Typ	Max	Units	Note
Erase to suspend	Sector erase or erase resume to erase suspend	700		µs	1
Program to suspend	Program resume to Program suspend	5		µs	1
Subsector erase to suspend	Subsector erase or subsector erase resume to erase suspend	50		µs	1
Suspend latency	Program	7		µs	2
Suspend latency	Subsector erase	15		µs	2
Suspend latency	Erase	15		µs	3

Note:
1. Timing is not internally controlled.
2. Any Read instruction accepted.
3. Any instruction except the following are accepted: Sector, Subsector, or Die Erase Write Status Register; Write Nonvolatile Configuration Register; and Program OTP.

Table 25. Operations Allowed/Disallowed During Device States
Note 1 applies to entire table

Operation	Standby State	Program or Erase State	Program Suspend State	Subsector Erase or Erase Suspend State	Note
Read	Yes	No	Yes	Yes	2
Program	Yes	No	No	Yes/No	3
Erase	Yes	No	No	No	4
Write	Yes	No	No	No	5
Write	Yes	No	Yes	Yes	6
Read	Yes	Yes	Yes	Yes	7
Suspend	No	Yes	No	No	8

Note:
1. The device can be in only one state at a time. Depending on the state of the device, some operations are allowed (Yes) and others are not (No). For example, when the device is in the standby state, all operations except Suspend are allowed in any sector. For all device states except the erase suspend state, if an operation is allowed or disallowed in one

sector, it is allowed or disallowed in all other sectors. In the erase suspend state, a Program operation is allowed in any sector except the one in which an Erase operation has been suspended.

2. All Read operations except Read Status Register and Read Flag Register. When issued to a sector or subsector that is simultaneously in an erase suspend state, the Read operation is accepted, but the data output is not guaranteed until the erase has completed.
3. All Program operations except Program OTP. In the erase suspend state, a Program operation is allowed in any Big Block (Yes) except the Big Block (No) in which an Erase operation has been suspended.
4. Applies to the Sector Erase or Subsector Erase operation.
5. Applies to the following operations: Write Status Register, Write Nonvolatile Configuration Register, Program OTP, and Die Erase.
6. Applies to the Write Volatile Configuration Register, Write Enhanced Volatile Configuration Register, Write Enable, Write Disable, Clear Flag Status Register, Write Extended Address Register, Enter 4-Byte Extended Address Register, Exit 4-Byte Extended Address Register, or Write Lock Register operation.
7. Applies to the Read Status Register or Read Flag Status Register operation.
8. Applies to the Program Suspend or Erase Suspend operation.

7.4.10 Program/Erase Resume (7AH)

The Program/Erase Resume instruction (7AH) must be written to resume the Subsector or Sector Erase operation or the Program operation after an Erase/Program Suspend. To initiate the Program/Erase Resume instruction, /CS is driven low. The instruction code is input on SI (for dual I/O protocol is IO0-IO1, quad I/O protocol is IO-IO3). The operation is terminated by driving /CS high, seeing ***Figure 109-Figure 110***.

When this instruction is executed, the status register write in progress bit is set to 1, and the flag status register Program erase controller bit is set to 0. This instruction is ignored if the device is not in a suspended state.

When the operation is in progress, the Program or erase controller bit of the flag status register is set to 0. The flag status register must be polled for the operation status. When the operation completes, that bit is cleared to 1. Note that the flag status register must be polled even if operation times out.

Figure 109. Program/Erase Resume (Extended SPI Mode)

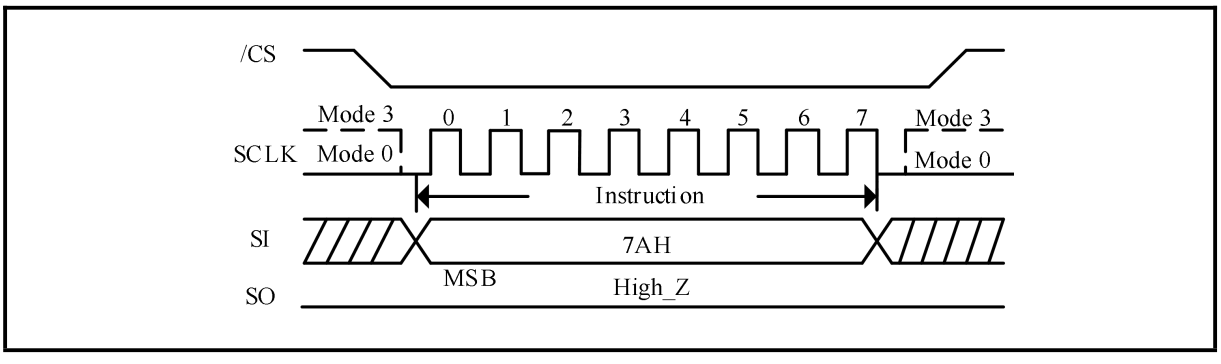
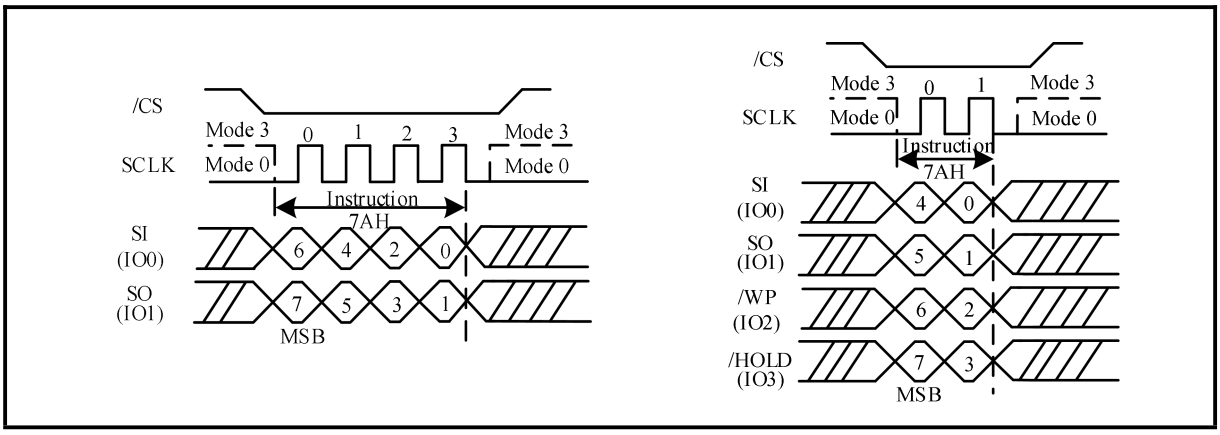


Figure 110. Program/Erase Resume (Dual/Quad I/O Mode)



7.5 OTP Operations

7.5.1 Read OTP Array (4BH)

See ***Figure 111-Figure 113,*** to initiate a Read OTP Array instruction, /CS is driven low. The instruction code is input on IO0/IO4 (for dual I/O protocol is IO0-IO1/IO4-IO5, quad I/O protocol is IO0-IO3/IO4-IO7), followed by address bytes and dummy clock cycles. Each address bit is latched in during the rising edge of clock. Data is shifted out on IO1/IO5 (for dual I/O protocol is IO0-IO1/IO4-IO5, quad I/O protocol is IO0-IO3/IO4-IO7), beginning from the specified address and at a maximum frequency of fC (MAX) on the falling edge of the clock. The address increments automatically to the next address after each byte of data is shifted out. There is no rollover mechanism; therefore, if Read continuously, after location 0x40, the device continues to output data at location 0x40. The operation is terminated by driving /CS high at any time during data output.

Figure 111. Read OTP Array Sequence Diagram (Extended SPI Mode)

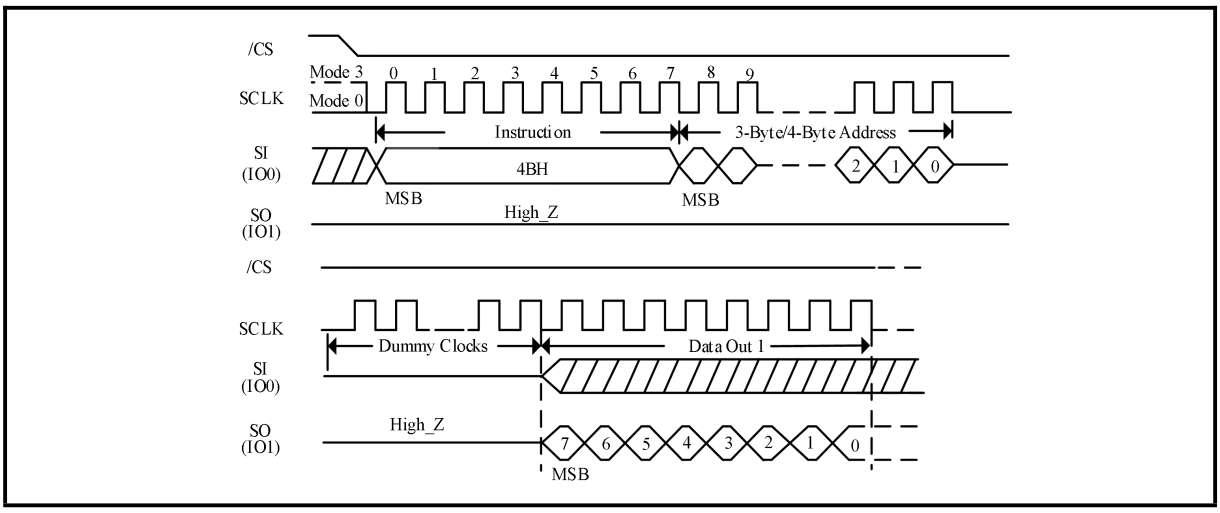


Figure 112. Read OTP Array Sequence Diagram (Dual I/O Mode)

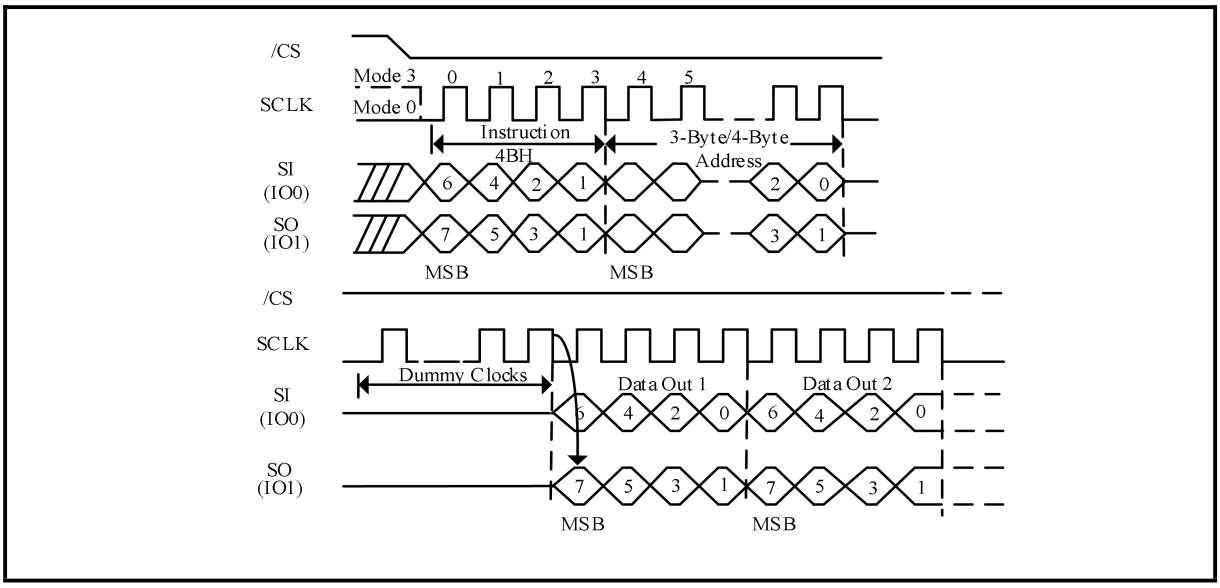
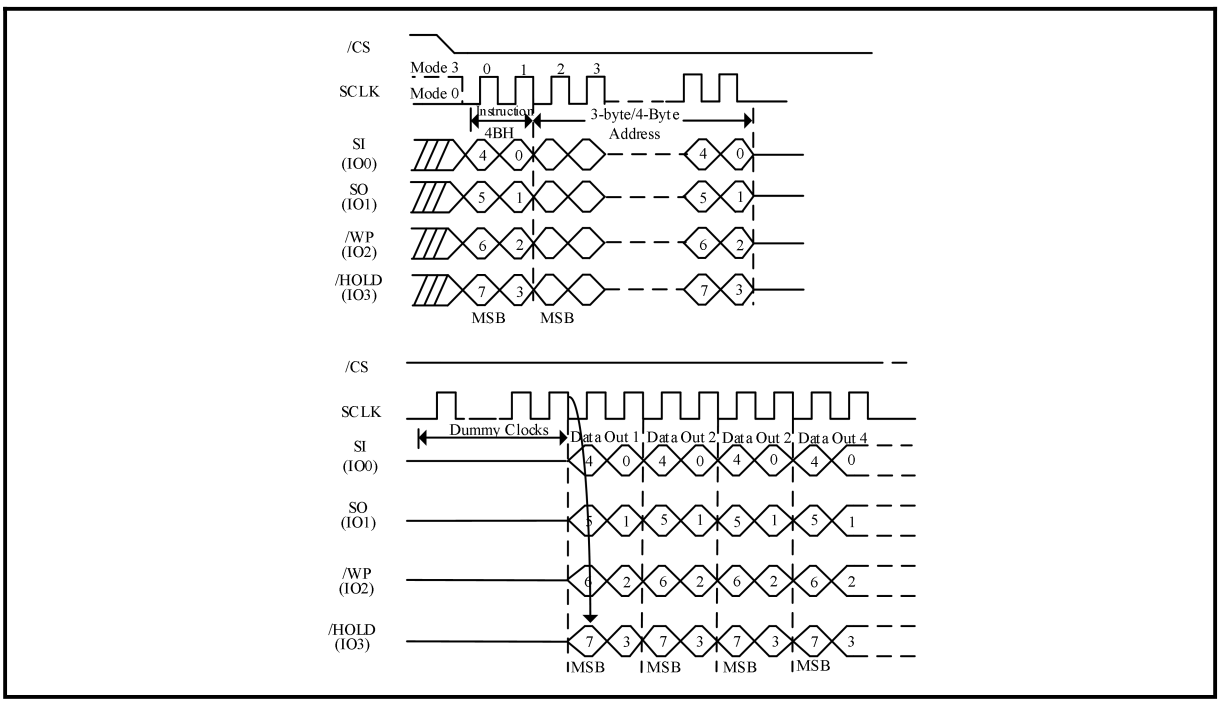


Figure 113. Read OTP Array Sequence Diagram (Quad I/O Mode)



Note:

1. The Read OTP Array instruction support 3-byte address and 4-byte address mode.
2. Dummy clock cycles can be set by the user through the Nonvolatile and Volatile Configuration Registers (See the ***Table 9*** and ***Table 10***).

7.5.2 Program OTP Array (42H)

See ***Figure 114-Figure 116***, to initiate the Program OTP Array instruction, the Write Enable instruction must be issued to set the write enable latch bit to 1; otherwise, the Program OTP Array instruction is ignored and flag status register bits are not set. /CS is driven low and held low until the eighth bit of the last data byte has been latched in, after which it must be driven high. The instruction code is input on IO0/IO4 (for dual I/O protocol is IO0-IO1/IO4-IO5, quad I/O protocol is IO0-IO3/IO4-IO7), followed by address bytes and at least one data byte. Each address bit is latched in during the rising edge of the clock. When /CS is driven high, the operation, which is self-timed, is initiated; its duration is tPP. There is no rollover mechanism; therefore, after a maximum of 65 bytes are latched in the subsequent bytes are discarded.

Program OTP Array Programs, at most, 64 bytes to the OTP memory area and one OTP control byte. When the operation is in progress, the write in progress bit is set to 1. The Write Enable Latch bit is cleared to 0, whether the operation is successful or not, and the status register and flag status register can be polled for the operation status. When the operation completes, the write in progress bit is cleared to 0.

If the operation times out, the Write Enable Latch bit is reset and the Program fail bit is set to 1. If /CS is not driven high, the instruction is not executed, flag status register error bits are not set, and the write enable latch remains set to 1. The operation is considered complete once bit 7 of the flag status register outputs 1 with at least one byte output.

The OTP control byte (byte 64) is used to permanently lock the OTP memory array, see ***Table 26***.

Table 26: OTP Control Byte (Byte 64)

Bit	Name	Settings	Description
0	OTP control byte	0 = Locked 1 = Unlocked(Default)	Used to permanently lock the 64-byte OTP array. When bit 0 = 1, the 64-byte OTP array can be Programmed. When bit 0 = 0, the 64-byte OTP array is Read only. Once bit 0 has been Programmed to 0, it can no longer be changed to 1. Program OTP array is ignored, the write enable latch bit remains set, and flag status register bits 1 and 4 are set.

Figure 114. Program OTP Array Sequence Diagram (Extended SPI Mode)

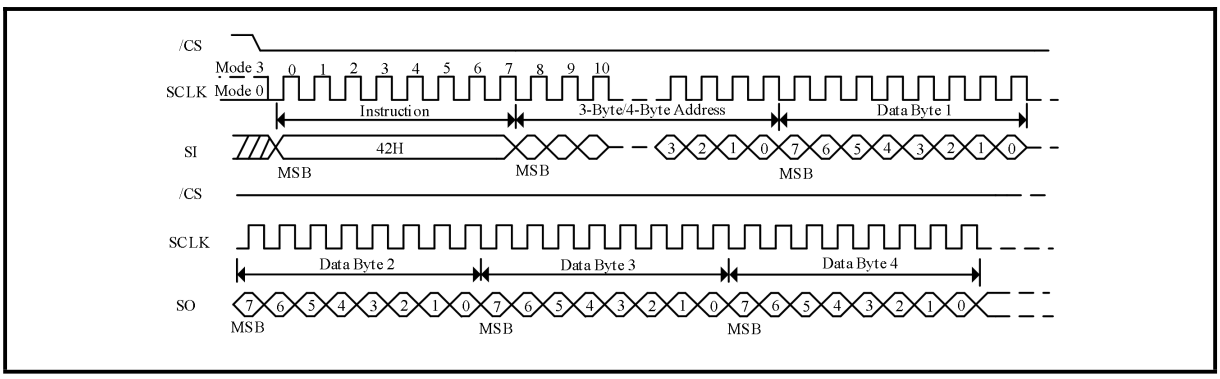


Figure 115. Program OTP Array Sequence Diagram (Dual I/O Mode)

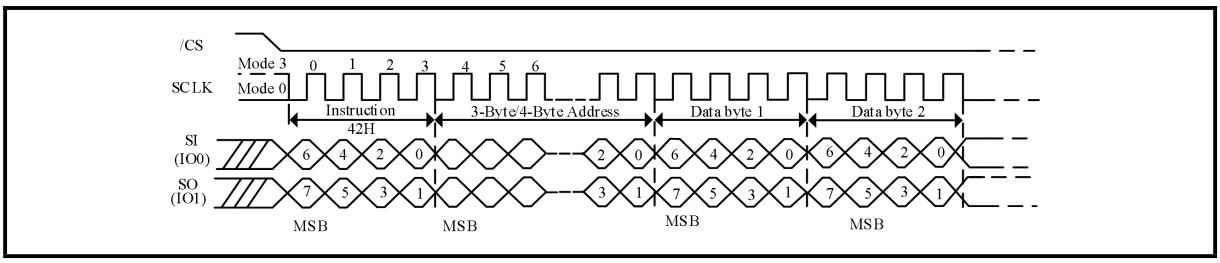
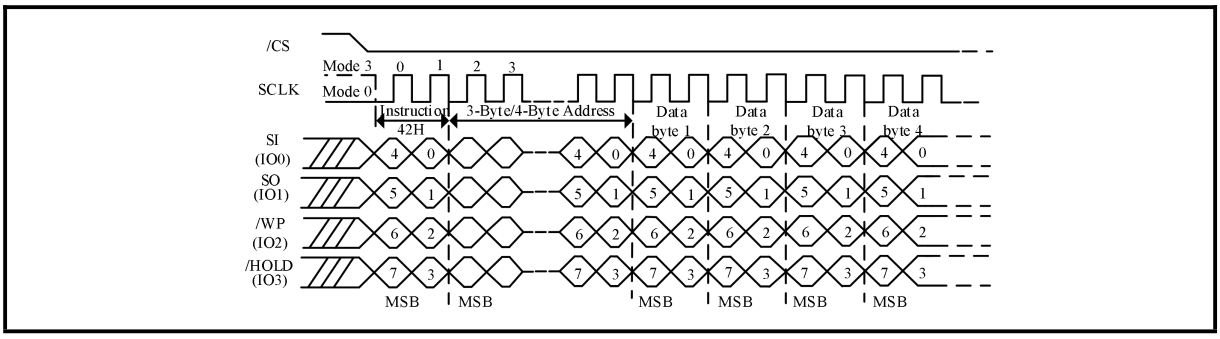


Figure 116.Program OTP Array Sequence Diagram (Quad I/O Mode)



Note:

1. The Program OTP Array instruction support 3-byte address and 4-byte address mode.
2.

8. Electrical Characteristics

8.1 Absolute Maximum Ratings

Parameter	Symbol	Conditions	Range	Unit.	Note
Supply Voltage	VCC		–0.6 to 4	V	
Voltage Applied to Any Pin	VIO	Relative to Ground	–0.6 to VCC + 0.6	V	3,4
Storage Temperature	TSTG		–65 to + 150	°C	
Electrostatic Discharge Voltage	VESD	Human Body Model	–2000 to + 2000	V	2
Fast program/erase voltage	VPP		–0.2 to 10	V	
Lead temperature during soldering	TLEAD		See note 1	°C	

Note:

1. Compliant with JEDEC Standard J-STD-020C (for small-body, Sn-Pb or Pb assembly), RoHS, and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU.
2. JEDEC Standard JESD22-A114A (C1 = 100pF, R1 = 1500Ω, R2 = 500Ω).
3. During signal transitions, minimum voltage may undershoot to –1V for periods less than 10ns.
4. During signal transitions, maximum voltage may overshoot to VCC + 1V for periods less than 10ns.

8.2 Operating Ranges

Parameter	Symbol	Conditions	Spec		Unit.
			Min	Max	
Supply Voltage	VCC		2.7	3.6	V
Supply voltage on VPP	VPPH		8.5	9.5	V
Temperature Operating	TA	Commercial	-40	+85	°C
		Industrial	-40	+85	

8.3 AC Reset Specifications

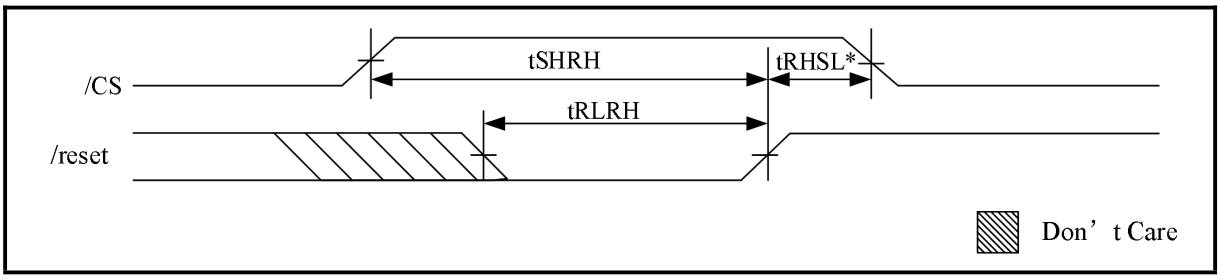
Note 1 applies to entire table

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Note
Reset pulse width	tRLRH2	50			ns		
Reset recovery time	tRHSL	Device deselected (/CS high) and is in XIP mode			40	ns	3
Device deselected (/CS high) and is in standby mode			40	ns			
Instructions are being decoded, any Read operations are in progress or any Write operation to volatile registers are in progress			40	ns			
Any device array Program/Erase/Suspend/Resume, Program OTP, Nonvolatile Sector Lock, and Erase Nonvolatile Sector Lock Array operations are in progress			30	µs			
While a Write Status Register operation is in progress		tW		ms			
While a Write Nonvolatile Configuration Register operation is in progress		tWNVCR		ms			
On completion or suspension of a Subsector Erase operation		tSSE		s			
Software reset recovery time	tSHSL3	Device deselected (/CS HIGH) and is in standby mode			40	ns	
Any Flash array Program / Erase / Suspend / Resume, Program OTP, Nonvolatile Sector Lock, and Erase Nonvolatile Sector Lock Array operations are in progress			30	µs			
While Write Status Register operation is in progress		tW		ms			
While a Write Nonvolatile Configuration Register operation is in progress		tWNVCR		ms			
On completion or suspension of a Subsector Erase operation		tSSE		s			
/CS deselect to reset valid	tSHRV	Deselect to reset valid in quad output or in QIO-SPI	2			ns	

Note:
1. Values are guaranteed by characterization; not 100% tested.
2. The device reset is possible but not guaranteed if tRLRH < 50ns.

3. In order to prevent the device from entering an unknown state, please do not send any instructions to the device during this period of time (tRHSL).

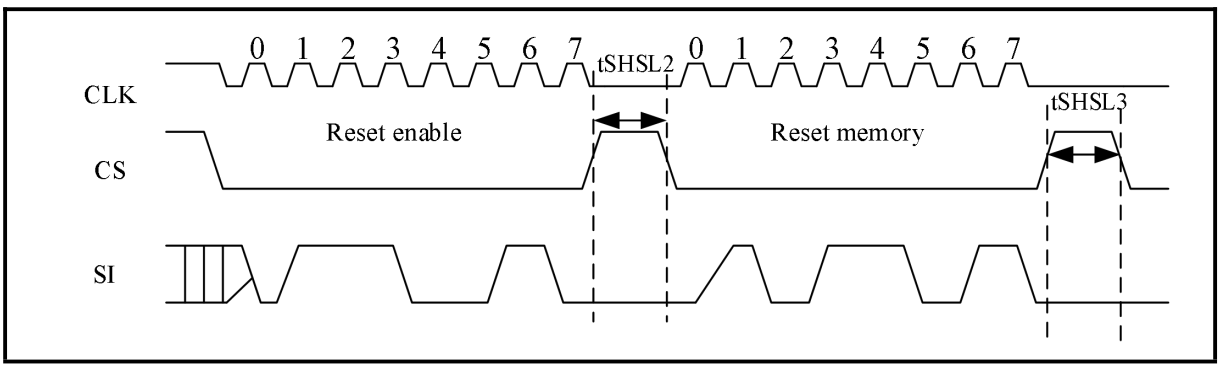
Figure 117. Reset AC Timing During PROGRAM or ERASE Cycle



Note:

1. In order to prevent the device from entering an unknown state, please do not send any instructions to the device during this period of time (tRHSL).

Figure 118. Reset Enable



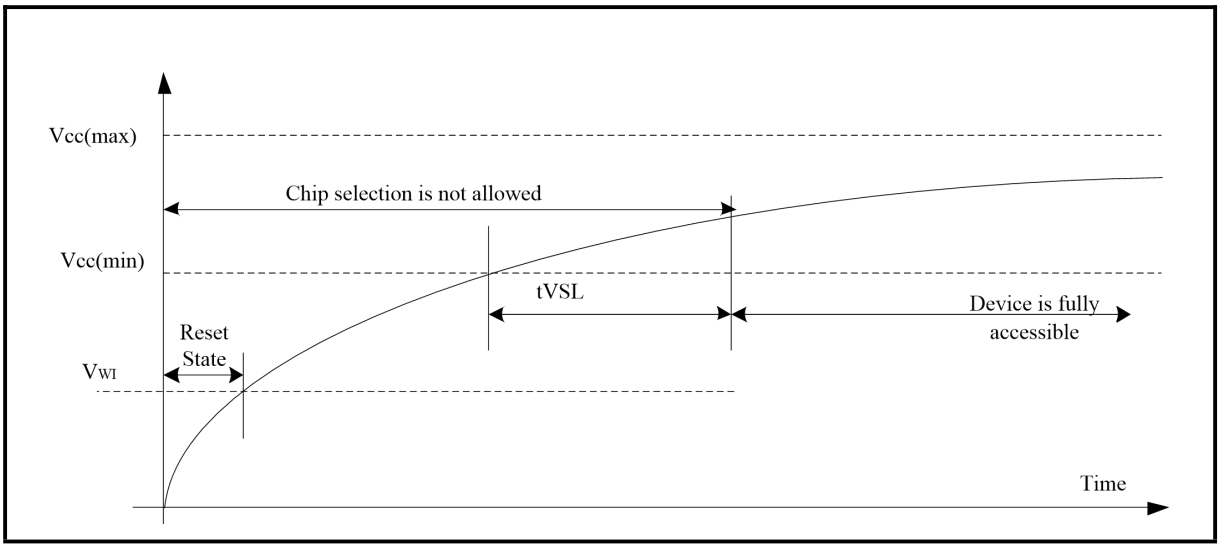
8.4 Latch Up Characteristics

Parameter	Min	Max
Input Voltage Respect To VSS On I/O Pins	-1.0V	VCC+1.0V
VCC Current	-100mA	100mA

8.5 Power-up Timing

Symbol	Parameter	Min	Max	Unit
tVSL	VCC(min) To /CS Low		150	us
V_{WI}	Write Inhibit Threshold Voltage V_{WI}	1.5	2.5	V

Figure 119. Power-up Timing and Voltage Levels



8.6 DC Electrical Characteristics

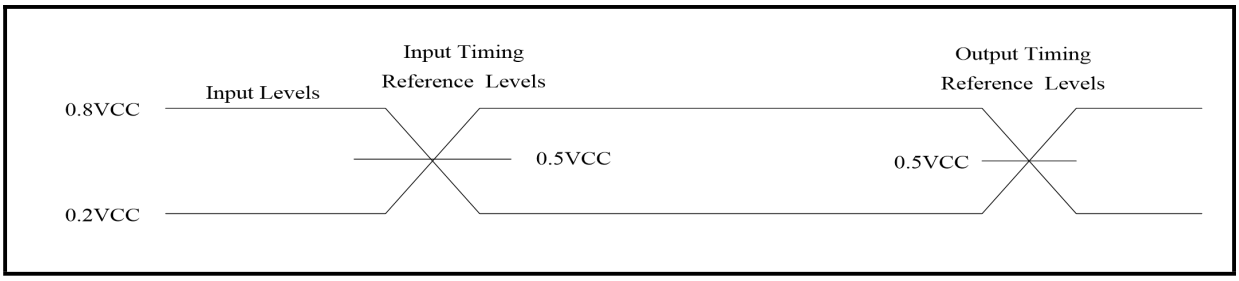
(T= -40℃~85℃, VCC=2.7~3.6V)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
ILI	Input Leakage Current				±2	μA
ILO	Output Leakage Current				±2	μA
ICC1	Standby Current	/CS=VCC, VIN=VCC or VSS			200	μA
ICC3	Operating current (fast-Read extended I/O)	C = 0.1VCC/0.9VCC at 108 MHz, DQ1 = open			15	mA
		C = 0.1VCC/0.9VCC at 54 MHz, DQ1 = open			6	mA
	Operating current (fast-Read dual I/O)	C = 0.1VCC/0.9VCC at 108 MHz			18	mA
	Operating current (fast-Read quad I/O)	C = 0.1VCC/0.9VCC at 108 MHz			20	mA
ICC4	Operating Current(Page Program)	/CS=VCC			20	mA
ICC5	Operating Current(write status register)	/CS=VCC			20	mA
ICC6	Operating Current(Subsector Erase)	/CS=VCC			20	mA
ICC7	Operating Current(Sector Erase)	/CS=VCC			20	mA
ICC8	Operating Current (Die Erase)	/CS=VCC			20	mA
VIL	Input Low Voltage		-0.5		0.3VCC	V
VIH	Input High Voltage		0.7VCC		VCC+0.4	V
VOL	Output Low Voltage	IOL =1.6mA			0.4	V
VOH	Output High Voltage	IOH =-100μA	VCC-0.2			V

8.7 AC Measurement Conditions

Symbol	Parameter	Min	Tpy.	Max	Unit.	Note
CL	Load Capacitance	30		30	pF	1
TR, TF	Input Rise And Fall time			5	ns	
VIN	Input Pause Voltage	0.2VCC to 0.8VCC			V	2
IN	Input Timing Reference Voltage	0.3VCC to 0.7VCC			V	
OUT	Output Timing Reference Voltage	0.5VCC			V	

Figure 120. AC Measurement I/O Waveform



8.8 AC Electrical Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit.	Note
Fc	Clock frequency for all instructions, except Read Data instruction (03H) & Read Data instruction with 4-Byte Address (13H) & DTR instructions	DC.		108	MHz	
fR	Clock freq. for Read Data instruction (03H), Read Data instruction with 4-Byte Address (13H)	DC.		55	MHz	
F_R	Clock freq. for DTR instructions	DC.		54	MHz	
tCLH	Serial Clock High Time	4			ns	
tCLL	Serial Clock Low Time	4			ns	1
tCLCH	Serial Clock Rise Time (Slew Rate)	0.1			V/ns	2,3
tCHCL	Serial Clock Fall Time (Slew Rate)	0.1			V/ns	2,3
tSLCH	/CS Active Setup Time	4			ns	
tCHSH	/CS Active Hold Time	4			ns	
tSHCH	/CS Not Active Setup Time	4			ns	
tCHSL	/CS Not Active Hold Time	4			ns	
tSHQZ	Output Disable Time			8	ns	
tCLQX	Output Hold Time	1			ns	
tDVCH	Data In Setup Time	2			ns	
tCHDX	Data In Hold Time	3			ns	
tHLCH	/Hold Low Setup Time (relative to Clock)	4			ns	
tHHCH	/Hold High Setup Time (relative to Clock)	4			ns	

Symbol	Parameter		Min.	Typ.	Max.	Unit.	Note
tCHHL	/Hold High Hold Time (relative to Clock)		4			ns	
tCHHH	/Hold Low Hold Time (relative to Clock)		4			ns	
tHLQZ	/Hold Low To High-Z Output				8	ns	
tHHQX	/Hold Low To Low-Z Output				8	ns	
tCLQV	Clock Low To Output Valid under 30pF	STR			8	ns	
		DTR			9	ns	
	Clock Low To Output Valid under 10pF	STR			6	ns	
		DTR			7	ns	
tWHSL	Write Protect Setup Time Before /CS Low		20			ns	4
tSHWL	Write Protect Hold Time After /CS High		100			ns	4
tESL	Erase Suspend Latency				30	µs	
tPSL	Program Suspend Latency				30	µs	
tPS	Latency between Program and next Suspend		20			µs	
tES	Latency between Erase and next Suspend		20			µs	
tPRS	Latency between Program Resume and next Suspend		20			µs	
tERS	Latency between Erase Resume and next Suspend		20			µs	
tW	Write Status Register Cycle Time			5	30	ms	
tWNVCR	Write Nonvolatile Configuration Register Time			5	30	ms	
tPP	Page Programming Time (256 byte)			0.5	5	ms	5
	Page Programming Time (n byte)			int(n/8) × 0.015[6]	5	ms	5
	Page Programming Time, VPP = VPPH (256 byte)			0.4	5	ms	5
	Program OTP Time (64 bytes)			0.2		ms	5
tSSE	Subsector Erase Time			0.25	0.8	s	
tSE	Sector Erase Time(64K Bytes)			0.7	3	S	
	Sector ERASE Time (with VPP = VPPH)			0.6	3	S	
tDSE	Die Erase Tim			240	480	S	
	Die Erase Time (with VPP = VPPH)			200	480	S	
tCFSR	Clear Flag Status Register Time			40		ns	
tWVCR	Write Volatile Configuration Register Time			40		ns	
tWRVECR	Write Volatile Enhanced Configuration Register Time			40			
tWREAR	Write Extended Address Register Time			40			
tVPPHSL	Enhanced VPPH high to /CS low for extended and dual I/O page program		200			ns	7
tSHSL1	/CS deselect time after a Read command		20			ns	
tSHSL2	/CS deselect time after a nonRead command		50			ns	

Note:

1. Typical values given for TA = 25 °C.

2. Tested with clock frequency lower than 50 MHz.
3. Expressed as a slew-rate.
4. Only applicable as a constraint for a Write Status REGISTER instruction when Status Register Write is set to 1.
5. When using the PAGE PROGRAM instruction to program consecutive bytes, optimized timings are obtained with one sequence including all the bytes versus several sequences of only a few bytes (1 < n < 256).
6. int(A) corresponds to the upper integer part of A. For example int(12/8) = 2, int(32/8) = 4 int(15.3) =16.
7. VPPH should be kept at a valid level until the PROGRAM or ERASE operation has completed and its result (success or failure) is known.

Figure 121. Serial input Timing

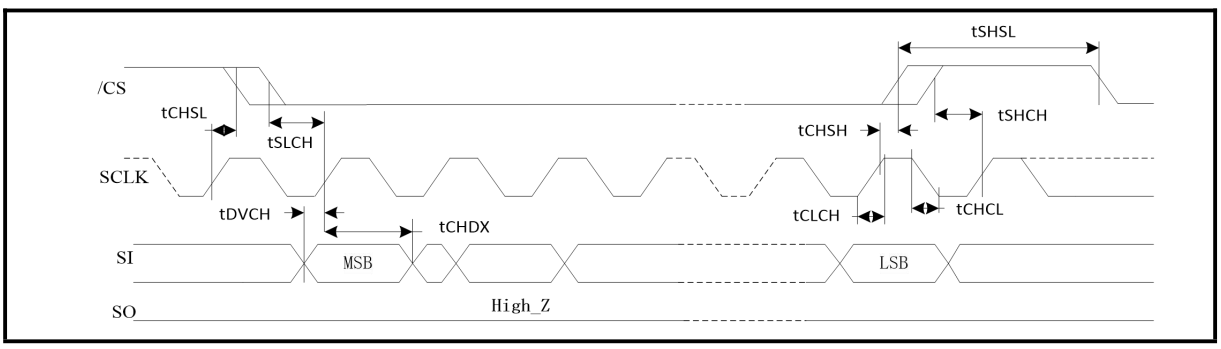


Figure 122. Output Timing

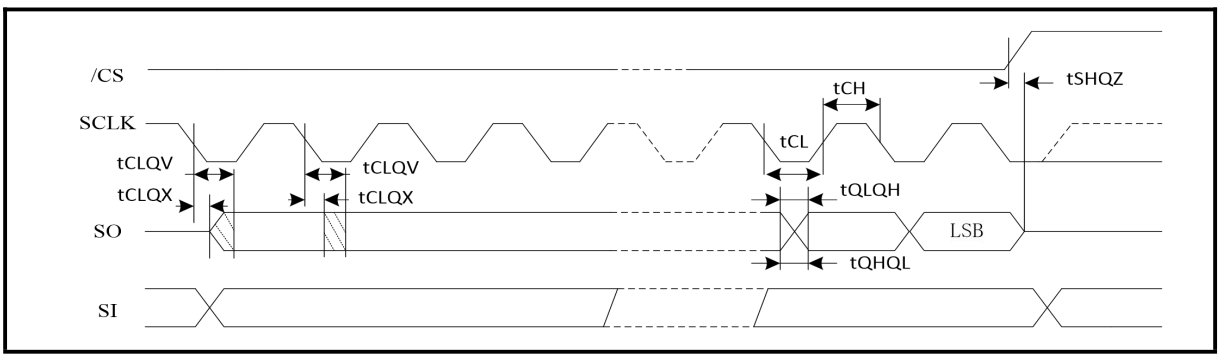


Figure 123. Hold Timing

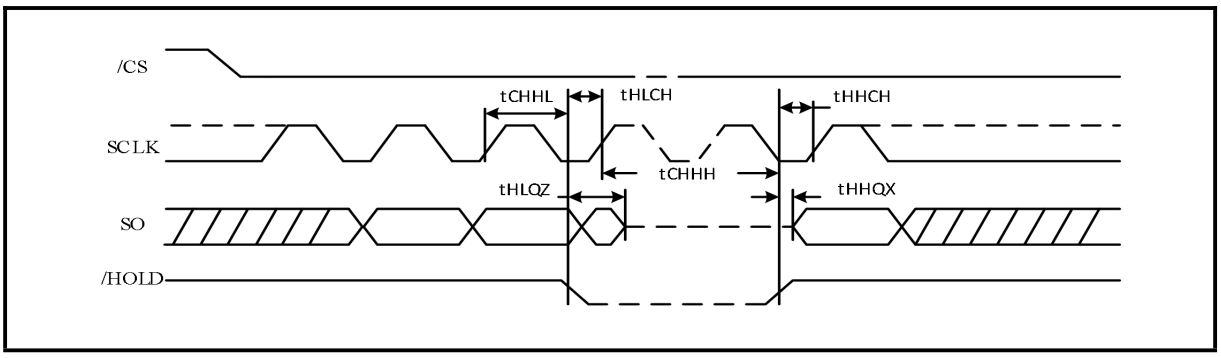


Figure 124. /WP Timing

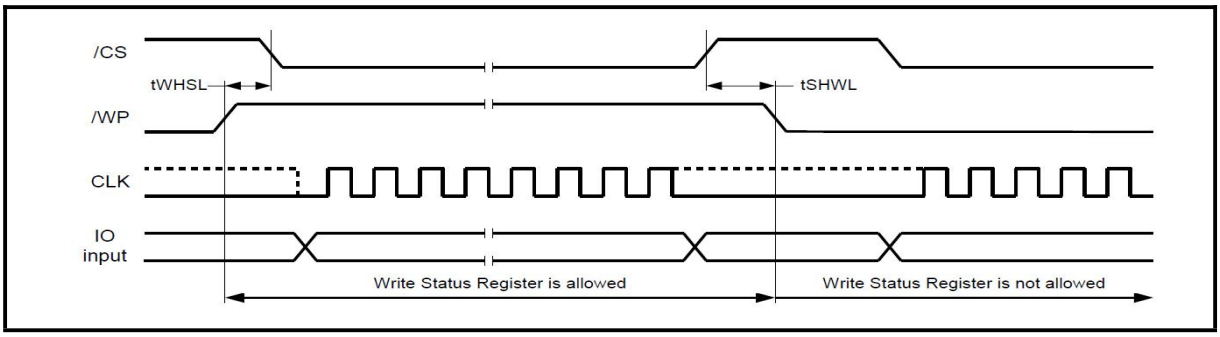
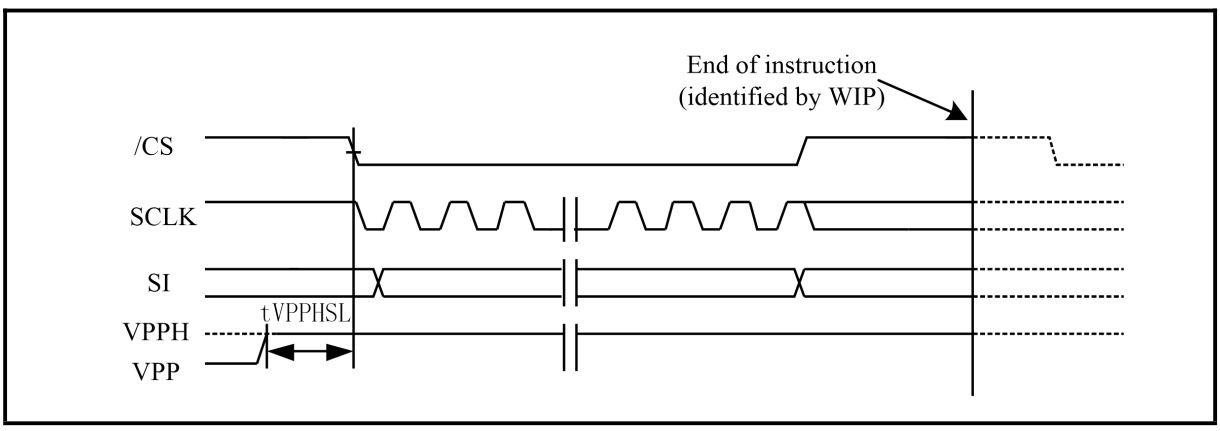
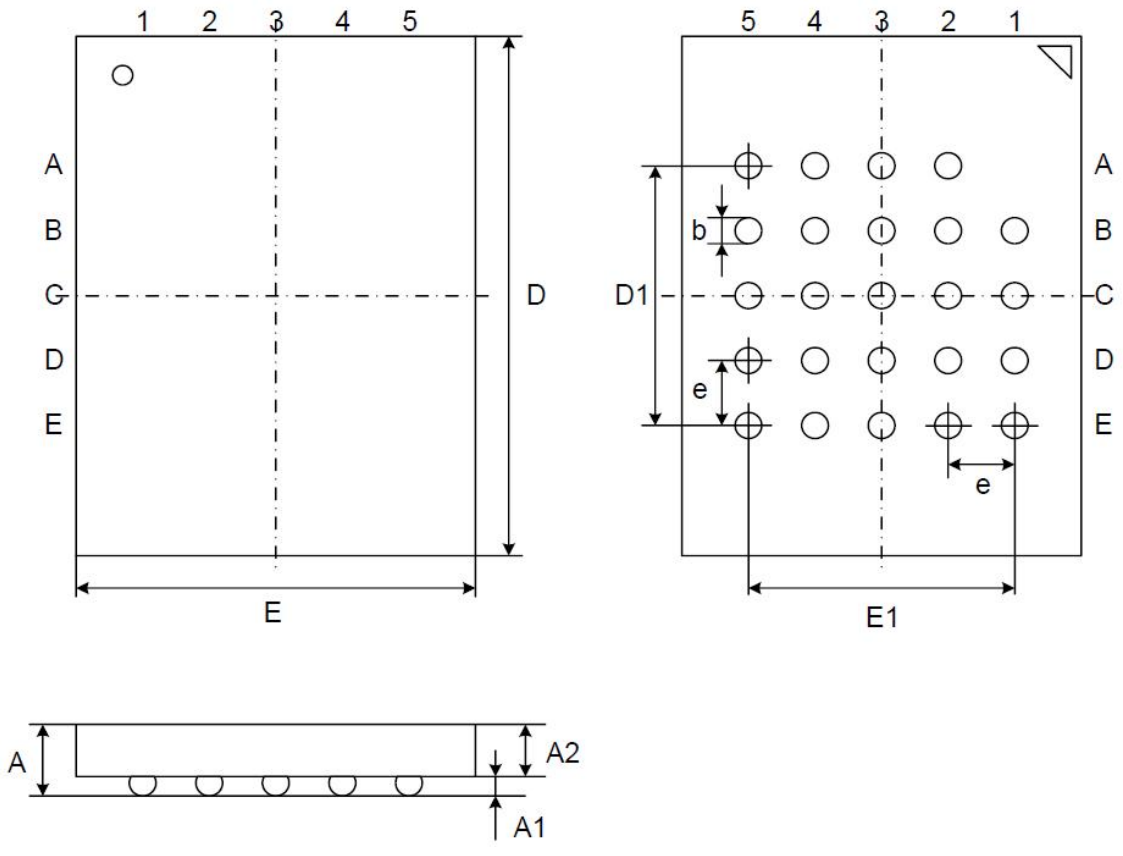


Figure 125. VPPH Timing



9. Package Information

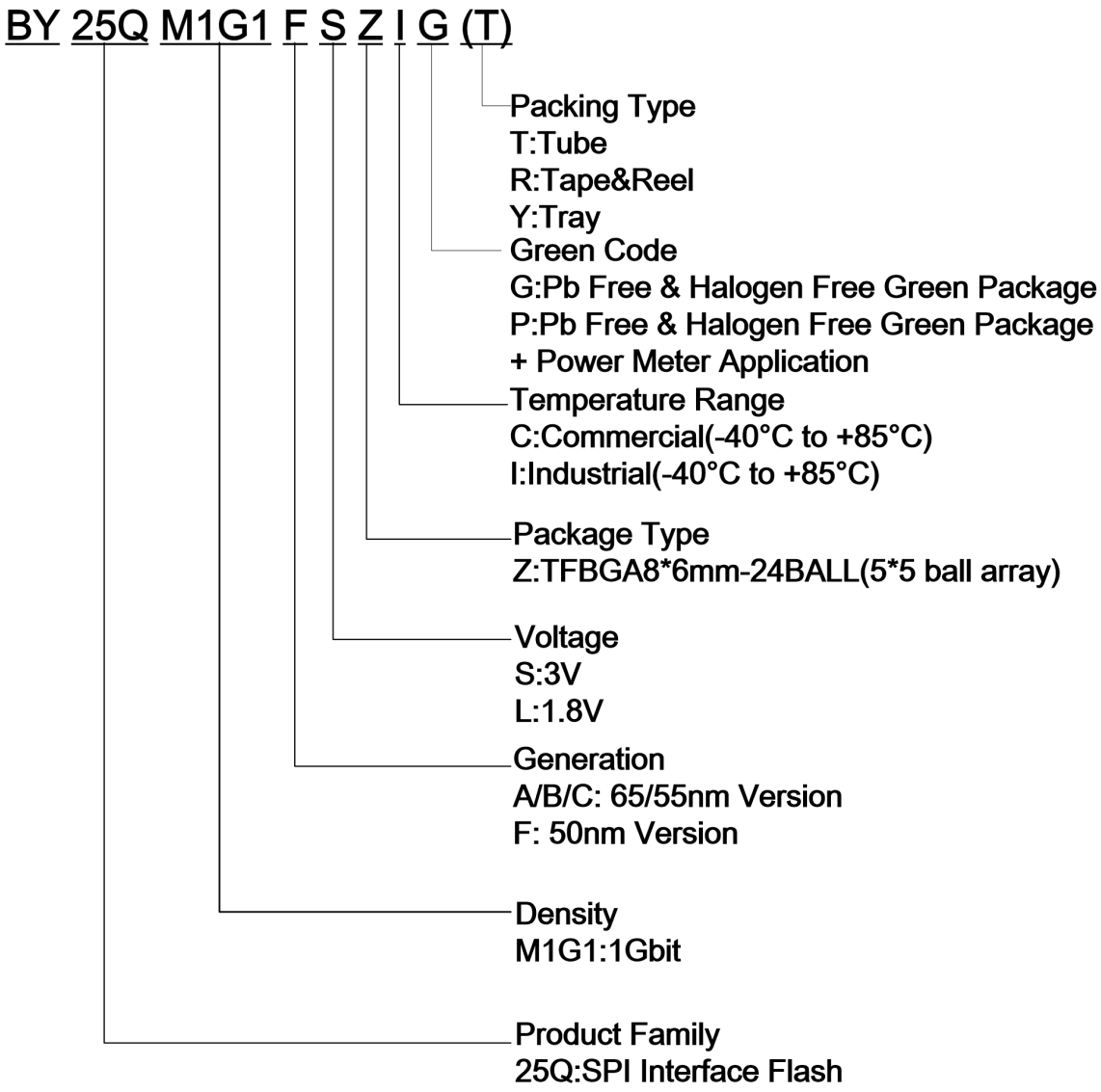
9.1 Package TFBGA8X6mm-24BALL (5X5 ball array)



Dimensions

Symbol / Unit		A	A1	A2	b	E	E1	D	D1	e
mm	Min	-	0.20	0.80	0.35	5.90	4.00	7.90	4.00	1.00
	Nom	-	0.25	0.85	0.40	6.00		8.00		
	Max	1.20	0.30	0.90	0.45	6.10		8.10		

10. Order Information



10.1 Valid part Numbers

The following table provides the valid part numbers for BY25QM1G1FS SPI Flash Memory. Pls contact BY Technology for specific availability by density and package type.

For consumer and industry application:

Package Type	Density	Product Number
Z TFBGA8X6mm-24BALL (5X5 ball array)	1G-bit	BY25QM1G1FSZIG

For Power Meter application:

Package Type	Density	Product Number
Z TFBGA8X6mm-24BALL (5X5 ball array)	1G-bit	BY25QM1G1FSZIP

10.2 Minimum Packing Quantity (MPQ)

Package Type	Packing Type	Qty for 1 Tube or Reel	Vacuum bag/ Inner Box	MPQ
TFBGA8X6mm-24BALL (5X5 ball array)	Tray	384ea/Tray	10+1 Trays/Bag 1Bag/InnerBox	3,840

11. Document Change History

REVISION	DATE	ORIGINATOR	DESCRIPTION
1.0	2020-09-10	Zuohuan Yu	Initiate; Based on BY25Q256FS_v1.8;
2.0	2020-11-29	Zuohuan Yu	Add *Part Number Information*;
3.0	2020-12-25	Zuohuan Yu	Modify VPP Accelerator bit description in *Enhanced Volatile Configuration Register Bit Definitions*;
4.0	2023-02-10	Zuohuan Yu	Update Commercial Temperature Range
4.1	2023-03-20	Zuohuan Yu	Update Package Information
4.2	2023-04-04	Zuohuan Yu	Update the logo and abbreviation

12. Appendix

12.1 Serial Flash Discovery Parameter Data Structure

Compliant with JEDEC standard JC-42.4 1775.03

Description		Address (Byte Mode)	Address (Bit)	Data
Serial Flash discoverable parameters signature		00H	7:0	53H
		01H	15:8	46H
		02H	23:16	44H
		03H	31:24	50H
Serial Flash discoverable parameters	Major revision	04H	7:0	00H
	Minor revision	05H	15:8	01H
Number of parameter headers		06H	7:0	00H
Reserved		07H	15:8	FFH
Parameter ID (0) JEDEC-defined parameter table		08H	7:0	00H
Parameter	Major revision	09H	15:8	00H
	Minor revision	0AH	23:16	01H
Parameter length (DW)		0BH	31:24	09H
Parameter table pointer		0CH	7:0	30H
		0DH	15:8	00H
		0EH	23:16	00H
Reserved		0FH	31:24	FFH

12.2 Parameter ID

Description	Byte Address	Bits	512Mb Data
Minimum block/sector erase sizes	30H	1:0	01b
Write granularity		2	1
Write Enable instruction required for writing to volatile status registers		3	0
Write Enable instruction selected for writing to volatile status registers		4	0
Reserved		7:5	111b
4KB Erase instruction	31H	7:0	20H
Supports Dual Output Fast Read operation (single input address, dual output)	32H	0	1
Number of address bytes used (3-byte or 4-byte) for array Read, Write, and Erase instructions		2:1	01b
Supports double transfer rate clocking		3	1
Supports Dual Input/Output Fast Read operation (dual input address, dual output)		4	1
Supports Quad Input/Output Fast Read operation (quad input address, quad output)		5	1
Supports Quad Output Fast Read operation (single input address, quad output)		6	1
Reserved		7	1
Reserved	33H	7:0	FFH
Flash size (bits)	34H	7:0	FFH
	35H	7:0	FFH

Description	Byte Address	Bits	512Mb Data
	36H	7:0	FFH
	37H	7:0	3FH
Number of dummy clock cycles required before valid output from Quad Input/Output Fast Read operation	38H	4:0	01001b
Number of XIP confirmation bits for Quad Input/Output Fast Read operation		7:5	001b
Instruction code for Quad Input/Output Fast Read operation	39H	7:0	EBH
Number of dummy clock cycles required before valid output from Quad Output Fast Read operation	3AH	4:0	00111b
Number of XIP confirmation bits for Quad Output Fast Read operation		7:5	001b
Instruction code for Quad Output Fast Rad operation	3BH	7:0	6BH
Number of dummy clock cycles required before valid output from Dual Output Fast Read operation	3CH	4:0	00111b
Number of XIP confirmation bits for Dual Output Fast Read operation		7:5	001b
Instruction code for Dual Output Fast Read operation	3DH	7:0	3BH
Number of dummy clock cycles required before valid output from Dual Input/Output Fast Read operation	3EH	4:0	00111b
Number of XIP confirmation bits for Dual Input/Output Fast Read		7:5	001b
Instruction code for Dual Input/Output Fast Read operation	3FH	7:0	BBH
Supports Fast Read operation in dual SPI protocol	40H	0	1
Reserved		3:1	111b
Supports Fast Read operation in quad SPI protocol		4	1
Reserved		7:5	111b
Reserved	43:41H	FFFFFFH	FFFFFFH
Reserved	45:44H	FFFFH	FFFFH
Number of dummy clock cycles required before valid output from Fast Read operation in dual SPI protocol	46H	4:0	00111b
Number of XIP confirmation bits for Fast Read operation in dual SPI protocol		7:5	001b
Instruction code for Fast Read operation in dual SPI protocol	47H	7:0	BBH
Reserved	49:48h	FFFFH	FFFFH
Number of dummy clock cycles required before valid output from Fast Read operation in quad SPI protocol	4AH	4:0	01001b
Number of XIP confirmation bits for Fast Read operation in quad SPI protocol		7:5	001b
Instruction code for Fast Read operation in quad SPI protocol	4BH	7:0	EBH
Sector type 1 size (4k)	4CH	7:0	0CH
Sector type 1 instruction code (4k)	4DH	7:0	20H
Sector type 2 size (64KB)	4EH	7:0	10H
Sector type 2 instruction code 64KB)	4FH	7:0	D8H
Sector type 3 size (not present)	50H	7:0	00H
Sector type 3 size (not present)	51H	7:0	00H
Sector type 4 size (not present)	52H	7:0	00H

Description	Byte Address	Bits	512Mb Data
Sector type 4 size (not present)	53H	7:0	00H

12.3 Part Number Information

Part Number Category	Category Details	Note
Feature set	1 = Byte addressability; HOLD pin; BY Technology XIP	1
	2 = Byte addressability; HOLD pin; Basic XIP	1
	3 = Byte addressability; RST# pin; BY Technology XIP	1
	4 = Byte addressability; RST# pin; Basic XIP	1
	5= Byte addressability; HOLD pin; BY Technology XIP	2

Note:

1. Enter 4-byte address mode and exit 4-byte address mode supported.
2. 4-byte addressing mode is the default at power-up. Enter and exit 4-byte addressing mode are not supported.